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This journal records developments in the application of electronics in science, industry, and the home. It contains information on the properties and performance of solid-state devices, valves and tubes, and associated components and assemblies. The practical circuits given are designed to provide the best working conditions and performance for the devices used. The design principles may be used (so far as device ratings allow) for adaptation to meet particular requirements. Current data should be consulted before any circuit is considered for production. Mullard Limited can normally supply only those devices or assemblies listed in the Company's current catalogues. Availability in quantity should be confirmed.

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Fast cycle switching and power-control system for use with transformer load controlled by three-phase fully-controlled a.c. controller

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UDC 621.316.728—558:621.3.025.3
621.382.333.4

This article describes a fast cycle switching and power-control system for switching transformer loads onto a three-phase mains supply without producing large inrush currents. The system consists of three main parts: a three-phase fully-controlled a.c. controller, an associated triggering system, and a slow-start and voltage-compensation circuit. The three-phase a.c. controller supplies a transformer load, and the associated triggering system is under the control of a slow-start circuit to ensure that when power is supplied to the load, the subsequent run-up to full power can be achieved in a minimum of time but without inrush current. The slow-start system also includes a circuit to compensate for changes in mains input voltage.

The trigger, slow-start, and voltage-compensation systems use 61-series circuit modules for ease of construction.

INTRODUCTION

A fast cycling and power-control system is described which allows a transformer load to be switched onto a three-phase mains supply without the formation of inrush currents. The phenomenon of inrush currents into a transformer, as a function of transformer loading conditions, position of the voltage waveform at switch-on, and core magnetisation conditions, is well described elsewhere (Ref. 1). This power control system is designed to allow fast cycling of the transformer without high current inrush.

The design described was to suit a particular requirement, but the system can be easily adapted to a range of cycling times and power transformer control requirements.

GENERAL DESCRIPTION OF SYSTEM

The basis of the system is the phase-angle-controlled and timed run-up to full power from a preset phase angle of a three-phase fully-controlled a.c. controller in the primary side of a transformer. The system specification was aimed to perform better than shown below:

approximately 300ms minimum full-load on period,
approximately 600ms minimum off period,
minimum run-up time of two to three cycles (40 to 60ms).

The application was in induction heating equipment where the requirements were:

1) cycle time approximately 30s,
2) on time approximately up to 15s,
3) run-up time approximately 5 cycles (100ms),
4) voltage stabilisation of load required to reduce the effect of mains variation,
5) power to be controlled 80kVA.

The control equipment comprises the following main components which are described in detail in the following sections:

1) three-phase fully-controlled a.c. controller,
2) triggering circuit,
3) run-up control circuit.

A.C. CONTROLLER

The circuit of the a.c. controller coupled to the primary of the three-phase transformer (excluding the slow-start and voltage-compensation circuits) is shown in Fig. 1. The transformer primary is in delta connection, with a star-connected secondary. For the purpose of experimental measurements, a nominal 5kVA, 380/120V delta/star transformer was used. Connection of the primary in delta gave a secondary phase-to-phase voltage of 205V which was fed into a 14Ω delta load.

The a.c. power controller was of the six-thyristor three-phase fully-controlled type. The transient suppression components have been omitted for simplicity in the a.c. controller circuit diagram Fig. 1, and would be incorporated according to the device ratings. The synchronising for the controller is in R-Y-B phase sequence, connected line-to-line. The synchronising and triggering logic gives an initial minimum trigger angle of about 30° at V_c=0V, and linear phase-angle control with V_c up to full conduction at approximately V_c=3·5V.

TRIGGER CIRCUIT

General description

The schematic circuit diagram of the printed-wiring trigger board is shown in Fig 2*. The 61-series thyristor trigger modules are used for the circuit functions. Three printed-wiring trigger boards are necessary for a three-phase a.c. controller system. The system operates on the following principle. A master trigger pulse train is gated to

*The phase control system and thyristor trigger circuit are a modification of the circuits designed for the d.c. motor reversible drive using regenerative braking described in Mullard Technical Communications, Vol. 12, No. 120, October 1973, pp 299 to 339.

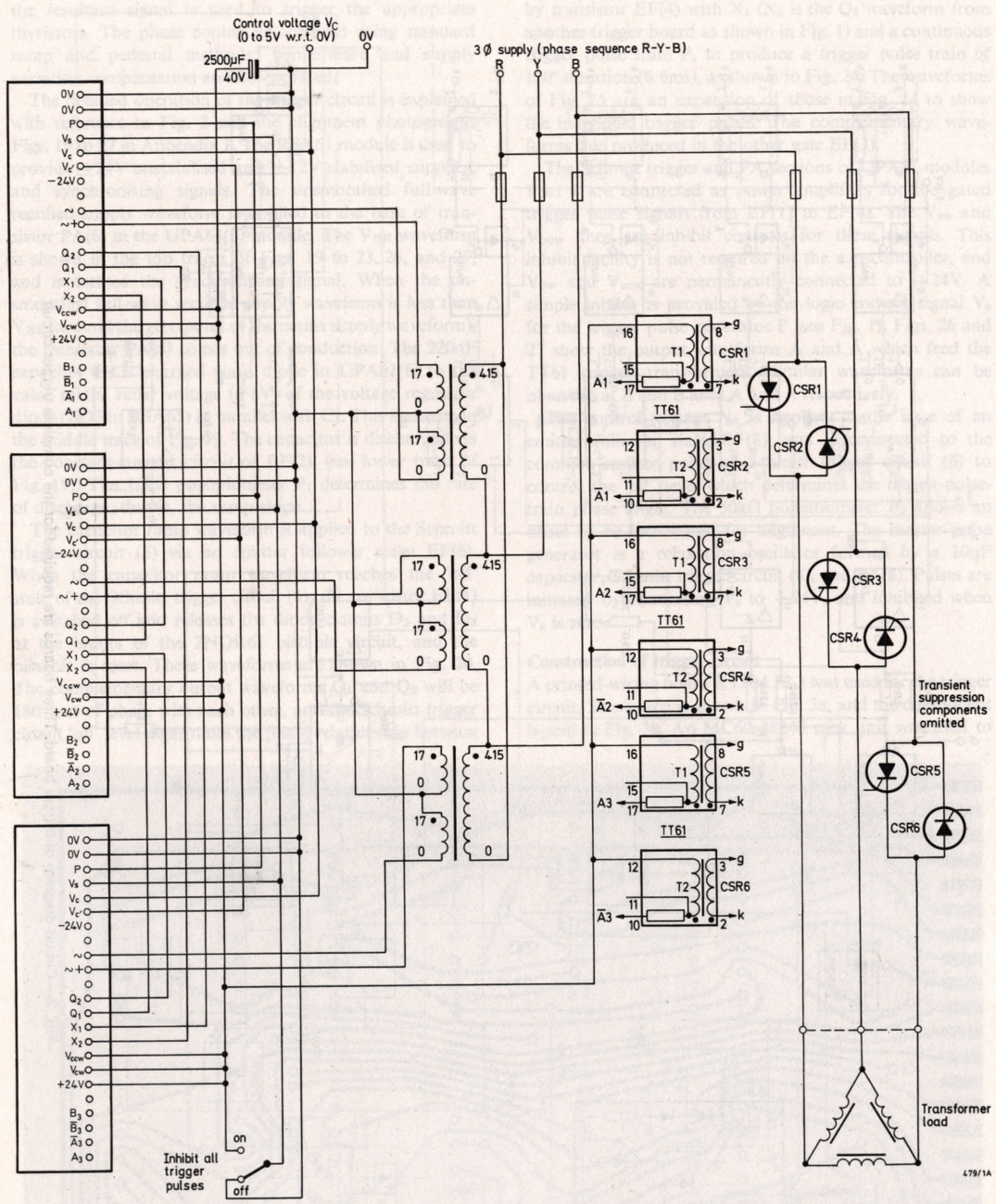

Fig. 1—Fast cycle switching and power-control system: three-phase fully-controlled a.c. controller and trigger circuit coupled into transformer primary winding

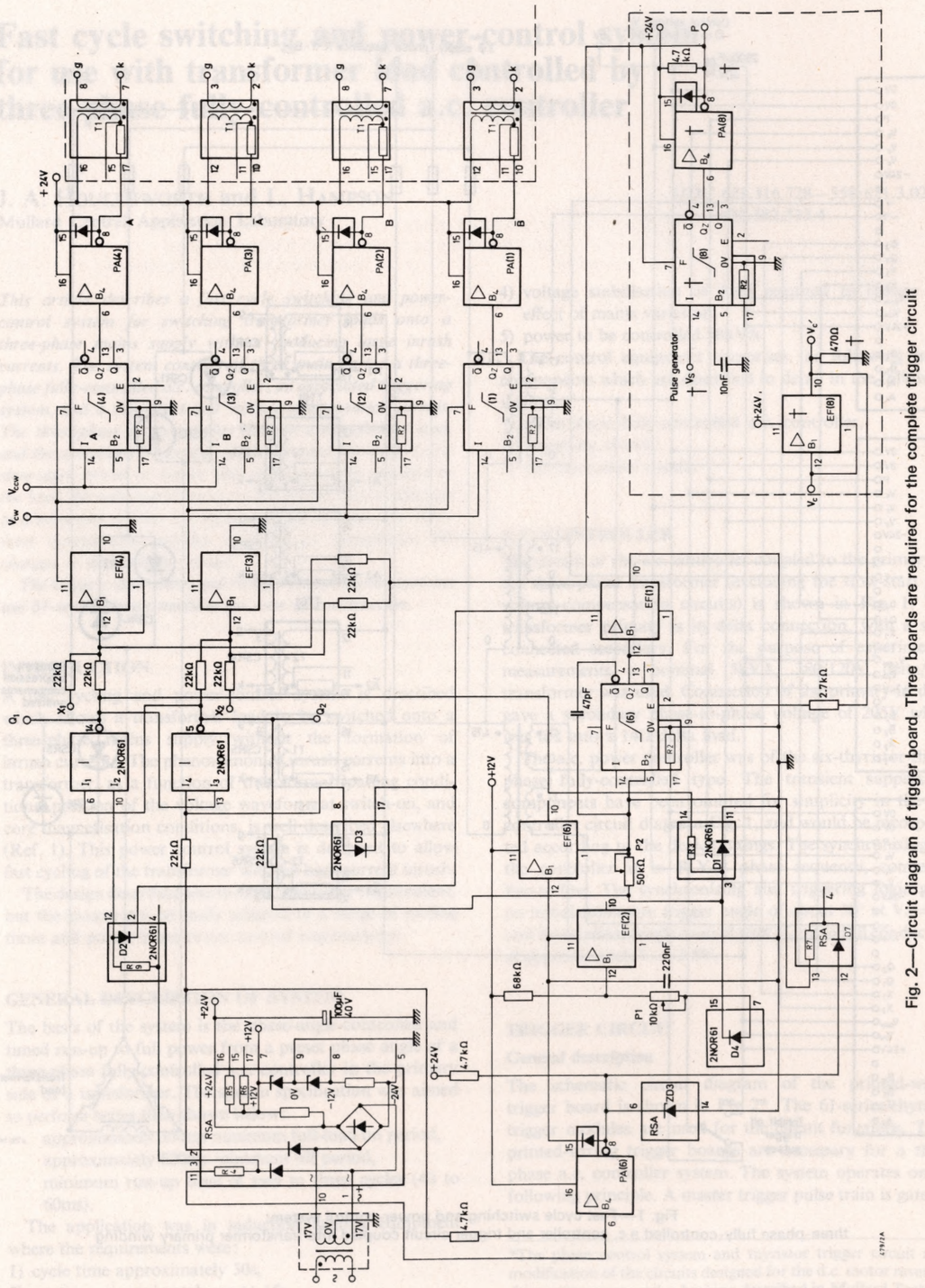

Fig. 2—Circuit diagram of trigger board. Three boards are required for the complete trigger circuit

a mains-synchronised internally-generated logic signal, and the resultant signal is used to trigger the appropriate thyristors. The phase control is achieved using standard ramp and pedestal methods; temperature and supply variation compensation are incorporated.

The detailed operation of the trigger circuit is explained with reference to Fig. 2 and the alignment photographs Figs. 19 to 27 in Appendix 1. The RSA61 module is used to provide ±24V unstabilised and +12V stabilised supplies, and synchronising signals. The unsmoothed full-wave rectified supply waveform is applied to the base of transistor PA(6) in the UPA61(6) module. The V_{BE} waveform is shown in the top traces of Figs. 19 to 23, 26, and 27, and is termed the synchronising signal. When the unsmoothed full-wave rectified supply waveform is less than V_{BE} (around the zero point of the mains supply waveform), the transistor PA(6) comes out of conduction. The 220nF capacitor C_1 is charged via a diode in UPA61(6) to the value of the zener voltage (6·8V) of the voltage regulator diode (ZD3 in RSA61) in parallel with C_1. This is shown in the middle trace of Fig. 19. The capacitor is discharged via the constant-current circuit of EF(2), (see lower trace of Fig. 19). The 10kΩ potentiometer P_1 determines the rate of discharge, that is, the ramp slope.

The capacitor ramp waveform is applied to the Schmitt trigger circuit (6) via an emitter follower stage EF(6). When the capacitor ramp waveform reaches the 'off' state of the Schmitt trigger circuit (6), the transistor EF(1) is switched off and releases the diode clamps D_2 and D_3 at the inputs of the 2NOR61 bistable circuit, and the bistable is reset. These waveforms are shown in Fig. 20. The complementary output waveforms Q_1 and Q_2 will be 180° out of phase with each other, and the Schmitt trigger circuit 'off' level determines the phase relationship between Q_1, Q_2, and the mains supply. The waveform Q_1 is gated by transistor EF(4) with X_1 (X_1 is the Q_1 waveform from another trigger board as shown in Fig. 1) and a continuous trigger pulse train P, to produce a trigger pulse train of 120° duration (6·6ms), as shown in Fig. 24. The waveforms of Fig. 25 are an expansion of those in Fig. 24 to show the individual trigger pulses. The complementary waveforms are produced in the other gate EF(3).

The Schmitt trigger and PA sections of UPA61 modules 1 to 4 are connected as power amplifiers for the gated trigger pulse signals from EF(1) to EF(4). The V_{cw} and V_{ccw} lines are inhibit controls for these signals. This inhibit facility is not required on the a.c. controller, and V_{cw} and V_{ccw} are permanently connected to +24V. A simple inhibit is provided by the logic control signal V_s for the trigger pulse generator P (see Fig. 1). Figs. 26 and 27 show the output waveforms A and Ā which feed the TT61 trigger transformers. Similar waveforms can be observed at B and B̄ as at A and Ā respectively.

The control voltage V_c is applied to the base of an emitter follower stage EF(8), and is connected to the common-emitter point of Schmitt trigger circuit (6) to control the 'off' level which determines the trigger-pulse-train phase angle. The 50kΩ potentiometer P_2 allows an offset to be introduced for alignment. The master pulse generator is a relaxation oscillator formed by a 10nF capacitor, Schmitt trigger circuit (8), and PA(8). Pulses are initiated by connecting V_s to +24V, and inhibited when V_s is zero.

Construction of trigger circuit

A printed-wiring board RT804.52.3 was used for the trigger circuit. The board is shown in Fig. 3a, and the component layout in Fig. 3b. An MC60 38240 rack unit was used to

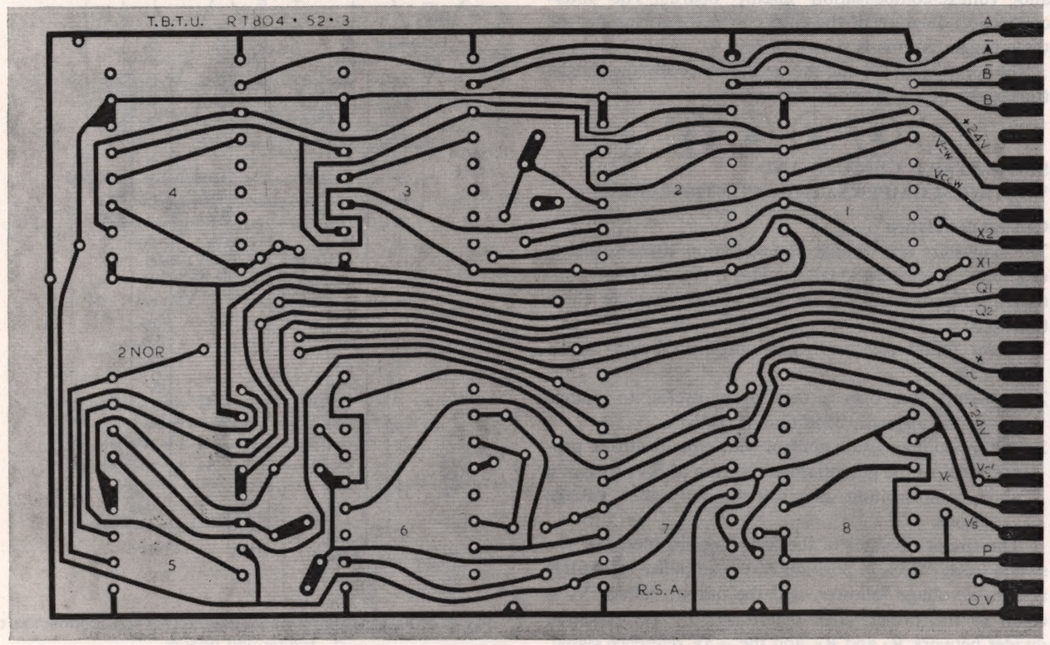

Fig. 3a—Printed-wiring board for trigger unit

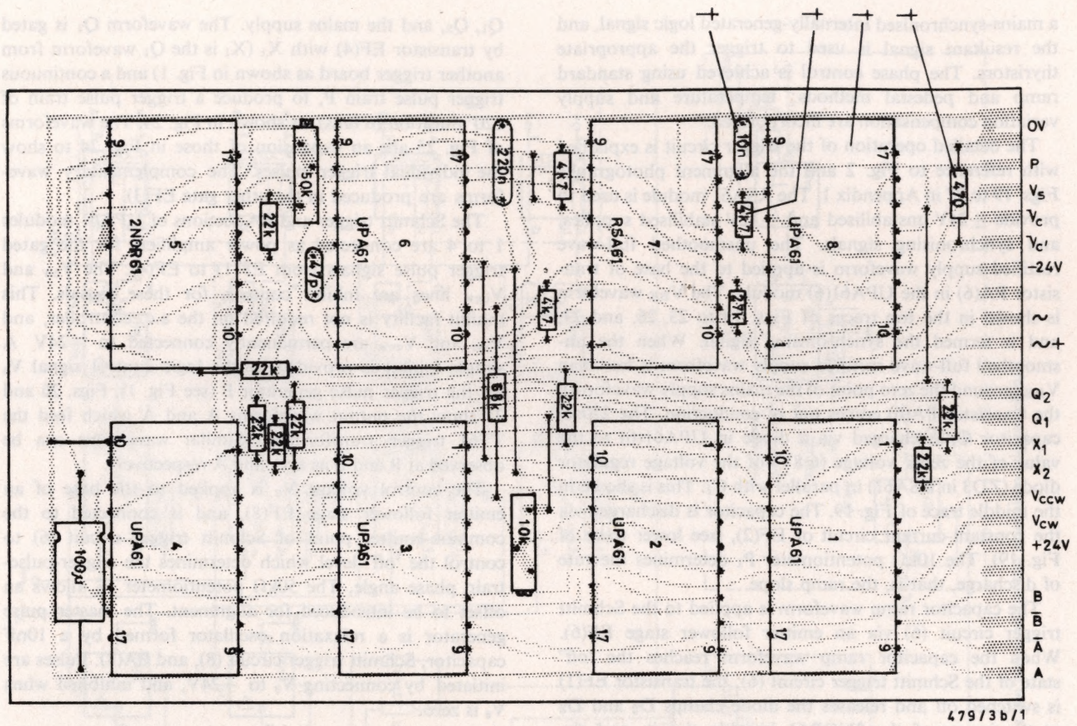

Fig. 3b—Component layout on printed-wiring board for trigger unit

accommodate the three trigger boards, and the slow-start and voltage-compensation circuit board. The interconnection diagram of the edge connector wiring for the three trigger boards is shown in Fig. 4.

The component list and the setting-up procedure for the trigger circuit are given in Appendix 1.

SLOW-START CIRCUIT AND VOLTAGE-COMPENSATION CONTROLLER

General description

The slow-start and voltage-compensation circuit consists of a number of operational amplifiers, type DOA61, connected as shown in Fig. 5. The circuit provides three functions:

1) preset initial step in trigger angle to avoid inrush currents,
2) slow-start run, over a number of cycles, to change slowly the magnetic condition of the core,
3) voltage-compensation control with error feedback proportional to the potentiometer setting of RV_1 to give a good compensation characteristic for mains voltage variations.

The circuit operates in the following manner. For the switch (relay) S_1/S_2 in position A, the amplifier DOA61(1) acts as a voltage follower, and the output voltage V_c is equal to the preset value determined by the potential divider network R_1 and R_2, and the +5V reference signal.

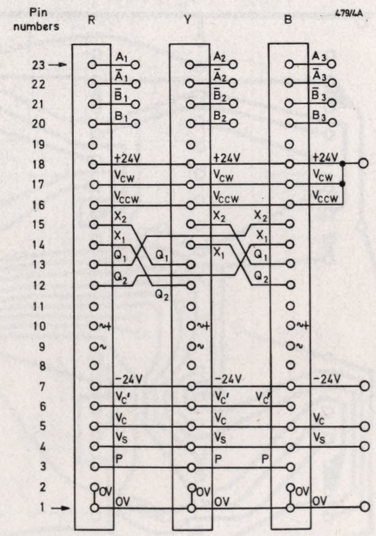

Fig. 4—Interconnection wiring diagram for edge connectors of trigger unit boards

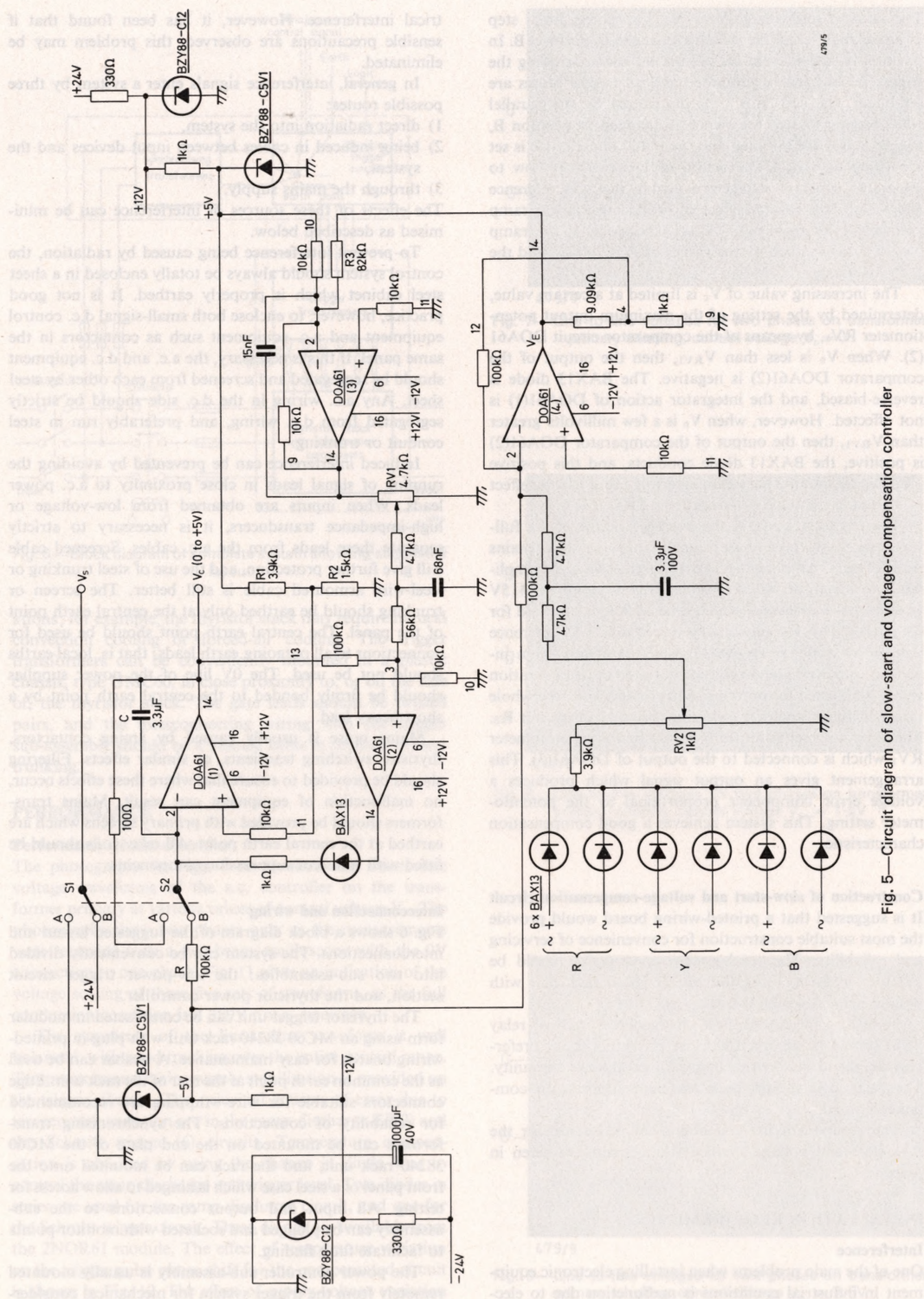

Fig. 5—Circuit diagram of slow-start and voltage-compensation controller

The value of this voltage $V_c = V_{step}$ gives the initial step in phase angle when the switch is changed to position B. In position A, the standby mode, the V_s line controlling the trigger pulse signal is grounded and all trigger pulses are inhibited. The capacitor C is discharged by the parallel 100Ω resistor. When the switch is changed to position B, trigger pulses are initiated and the initial phase angle is set according to V_{step}. The action of DOA61(1) is now to integrate a constant voltage provided by the −5V reference and V_{step}. This has the effect of producing a linear ramp voltage for V_c from $V_c = V_{step}$. The slope of the ramp dV_c/dt is determined by the values of R, C, V_{step}, and the −5V reference.

The increasing value of V_c is limited at a certain value, determined by the setting of the maximum output potentiometer RV_1, by means of the comparator circuit DOA61(2). When V_c is less than V_{RV1}, then the output of the comparator DOA61(2) is negative. The BAX13 diode is reverse-biased, and the integrator action of DOA61(1) is not affected. However, when V_c is a few millivolts greater than V_{RV1}, then the output of the comparator DOA61(2) is positive, the BAX13 diode conducts, and this positive input signal into the high-gain inverting input has the effect of clamping the output voltage from DOA61(1).

The feedback signal is the average voltage of the full-wave rectified three-phase signal from the 17V mains transformers. Amplifier DOA61(4) acts as an error amplifier with a gain of 100. At nominal mains supply of 415V U.K. (380V European), potentiometer RV_2 is adjusted for 0V output. This voltage signal is added to a +5V reference voltage in amplifier DOA61(3) which is a unity gain inverting amplifier. The magnitude of the error compensation signal is adjusted for optimum performance over the whole range of trigger angles by selecting the value of resistor R_3. The maximum set point for V_c is set by the potentiometer RV_1 which is connected to the output of DOA61(3). This arrangement gives an output signal which produces a voltage error component proportional to the potentiometer setting. This system achieves a good compensation characteristic.

Construction of slow-start and voltage-compensation circuit

It is suggested that a printed-wiring board would provide the most suitable construction for convenience of servicing and reliability. The total system construction could be modular in form, using the MC60 38240 rack unit with plug-in printed-wiring boards.

Note that the double-pole changeover switch or relay S_1/S_2 should be mounted in close proximity to, or preferably on, the printed-wiring board for good noise immunity. The relay coil should have transient suppression components fitted.

The component list and alignment procedure for the slow-start and voltage-compensation circuit are given in Appendix 2.

INSTALLATION REQUIREMENTS

Interference

One of the main problems when installing electronic equipment in industrial conditions is malfunction due to electrical interference. However, it has been found that if sensible precautions are observed, this problem may be eliminated.

In general, interference signals enter a system by three possible routes:

1) direct radiation into the system,
2) being induced in cables between input devices and the system,
3) through the mains supply.

The effects of these sources of interference can be minimised as described below.

To prevent interference being caused by radiation, the control system should always be totally enclosed in a sheet steel cabinet which is properly earthed. It is not good practice, however, to enclose both small-signal d.c. control equipment and a.c. equipment such as contactors in the same panel. If this is necessary, the a.c. and d.c. equipment should be segregated and screened from each other by steel sheet. Any a.c. wiring in the d.c. side should be strictly segregated from d.c. wiring, and preferably run in steel conduit or trunking.

Induced interference can be prevented by avoiding the running of signal leads in close proximity to a.c. power leads. When inputs are obtained from low-voltage or high-impedance transducers, it is necessary to strictly separate these leads from the a.c. cables. Screened cable will give further protection, and the use of steel trunking or steel-wire armoured cable is still better. The screen or trunking should be earthed only at the central earth point of the panel. The central earth point should be used for connections to all outgoing earth leads; that is, local earths should not be used. The 0V line of the power supplies should be firmly bonded to the central earth point by a short heavy lead.

Mains noise is usually caused by arcing contactors, thyristor switching transients, or similar effects. Filtering should be provided to ensure that where these effects occur, no malfunction of equipment can result. Mains transformers should be provided with primary screens which are earthed at the central earth point. All relay coils should be fitted with transient suppression components.

Interconnection and wiring

Fig. 6 shows a block diagram of the suggested layout and interconnections. The system can be conveniently divided into two sub-assemblies: the low-power trigger circuit section, and the thyristor power controller.

The thyristor trigger unit can be constructed in modular form using an MC60 38240 rack unit with plug-in printed-wiring boards for easy maintenance. A busbar can be used as the common earth point at the rear of the rack unit. Edge connectors suitable for wire-wrapping are recommended for reliability of connections. The synchronising transformers can be mounted on the end plate of the MC60 38240 rack unit, and the rack can be mounted onto the front panel of a steel case which is hinged to allow access for testing. All input and output connections to the sub-assembly can be plugged and socketed with monitor points to facilitate fault finding.

The power controller sub-assembly is usually mounted remotely from the trigger system for mechanical considerations; for example, the thyristor stack may require natural convection cooling or forced-air cooling. The trigger transformers can be conveniently mounted in a plastic chassis, type UMC60, in close proximity to, or on the side of, the thyristor stack. The gate leads should be twisted pairs, and the interconnecting wiring with the trigger sub-assembly should be a loomed cable in conduit or steel trunking.

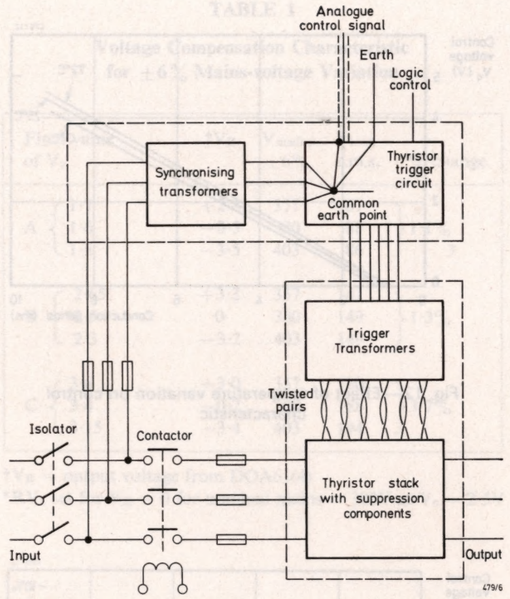

Fig. 6—Block diagram of complete system showing suggested layout

PERFORMANCE

Performance of a.c. controller

The photographs in Figs. 7 to 11 show the line-to-line voltage waveforms of the a.c. controller on the transformer primary at various values of control voltage V_c. The photographs show two phases only as the measurements were recorded with a two-beam oscilloscope with the 0V connection to one phase. Fig. 11 gives an indication of the voltage scaling of these five sets of waveforms, as the full conduction condition is a 380V r.m.s. sinewave.

The symmetry of the line-to-line waveform is well balanced, with good tracking over the entire control range. Temperature and mains supply stabilisation is provided on the trigger circuits. The principal sources of error due to temperature variation are in the ramp discharge EF(2) and the Schmitt trigger (6) circuits. Temperature compensation is obtained by using the change in diode V_{BE} to control the ramp discharge and trigger level. Two diodes in series are used for the ramp discharge circuit, and one for the Schmitt trigger circuit. These diodes are available from the 2NOR61 module. The effect of temperature variation on the trigger pulse phase shift for the compensated circuit is shown in Fig. 12. The effect of supply-voltage variation

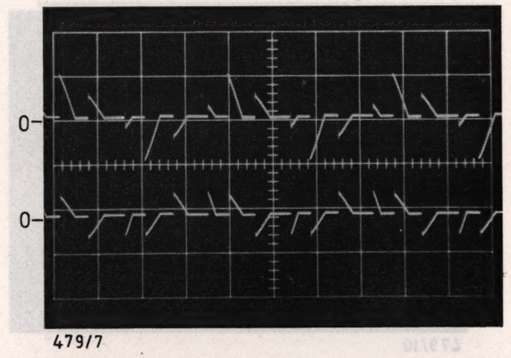

Fig. 7—Line-to-line voltages for two phases on transformer primary winding, control voltage $V_c = 0$

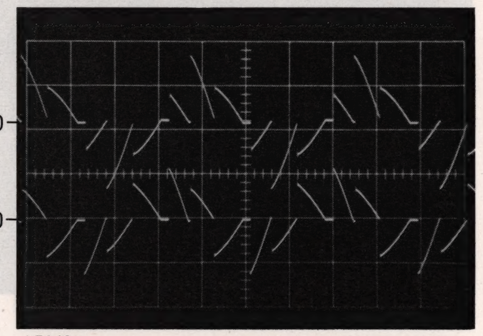

Fig. 8—Line-to-line voltages for two phases on transformer primary winding, control voltage $V_c = 1{\cdot}5V$

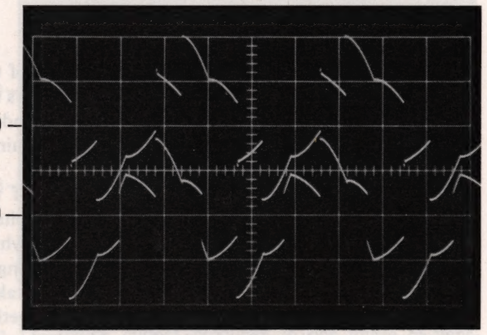

Fig. 9—Line-to-line voltages for two phases on transformer primary winding, control voltage $V_c = 2{\cdot}5V$

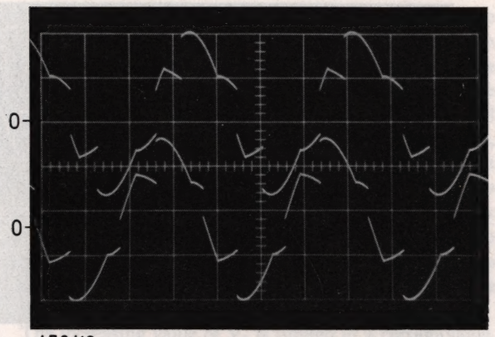

Fig. 10—Line-to-line voltages for two phases on transformer primary winding, control voltage $V_c = 3{\cdot}0V$

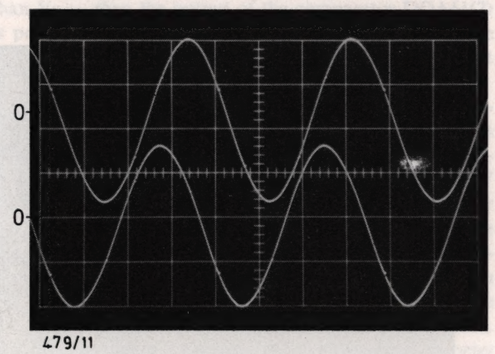

Fig. 11—Line-to-line voltages for two phases on transformer primary winding, control voltage $V_c = 3{\cdot}5V$

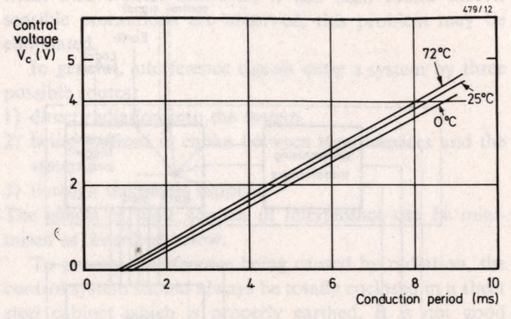

Fig. 12—Effect of temperature variation on control characteristic

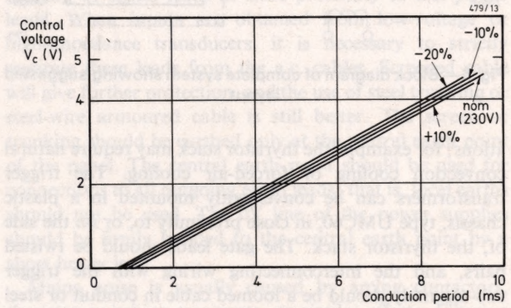

Fig. 13—Effect of mains voltage variation on control characteristic

in the control characteristic is shown in Fig. 13. In Figs. 12 and 13, the effects of temperature have been reduced to small variations.

Performance of slow-start circuit and voltage-compensation controller

The photograph in Fig. 14 shows the characteristic of the linear ramp of the slow-start run-up circuit. This shows the pre-step voltage, and the run-up to final voltage dependent on the setting of RV_1. These characteristics were obtained using a storage oscilloscope.

The results in Table 1 show the performance of the voltage-compensation system for a $\pm 6\%$ mains voltage variation. Three sets of figures are given, A, B, and C which correspond to low, medium, and high conduction angles in the a.c. controller after the run-up condition has taken place. The final value of V_c is given in Table 1, together with the corresponding r.m.s. load voltage. Nominal mains input is shown as 380V r.m.s. As the mains voltage value is varied up to $\pm 6\%$, the change in load voltage varies $1{\cdot}1\%$,

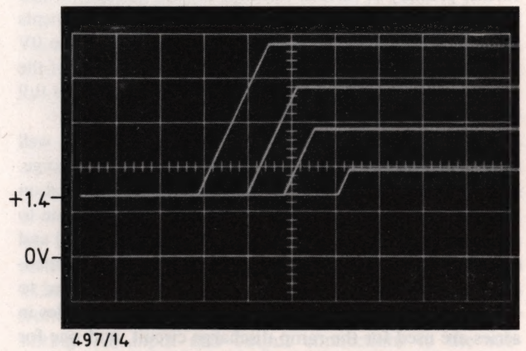

Fig. 14—Slow-start circuit operation:
V_c characteristic for different RV_1 set points
Vertical scale: 1V per main division
Horizontal scale: 100ms per main division

TABLE 1

Voltage Compensation Characteristic for $\pm 6\%$ Mains-voltage Variation

	Final value of V_c	†V_E	V_{mains} $\pm 6\%$	V_{load} r.m.s.	% change
A	1·7	+2·8	357	87	1·1%
	1·6	−0·5	380	88	
	1·5	−3·5	403	86	
B	2·65	+3·2	357	147	1·3%
	*2·5	0	380	149	
	2·3	−3·2	403	149	
C	3·6	+3·0	357	180	3·7%
	3·4	−0·2	380	188	
	3·15	−3·4	403	194	

†V_E = output voltage from DOA61(4)
*RV_2 set for $V_E = 0$ for nominal mains = 380V at $V_c = 2{\cdot}5V$

1·3%, and 3·7% for low, medium, and high conduction angles respectively. The error voltage V_E at the output of the amplifier DOA61(4) is also included.

Performance of complete system

The run-up performance of the complete system is illustrated by the photographs in Figs. 15 and 16. The waveforms shown indicate the currents flowing in two phases of the delta-connected primary winding. The current waveforms were obtained by inserting a $0{\cdot}1\Omega$ resistor in each phase of the primary winding.

Fig. 15 shows the current waveform for an initial V_c of 1·4V to a final V_c of 3·0V. Fig. 16 indicates a similar initial start voltage, but with a final value of V_c of 3·5V, giving full conduction in the a.c. controller. The run-up condition shown in the photographs occupies some three to four cycles of mains period, and it will be seen that there is a complete absence of excessive inrush currents.

The photograph of Fig. 17 illustrates the formation of an inrush current in one of the phases when the run-up time is too short, in this case about one half-cycle of mains period.

The system has been tested and designed for a specific requirement in a 80kVA induction heating equipment. The equipment performed very satisfactorily.

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1. STIGANT, S. A. and FRANKLIN, A. C. 'The J & P Transformer Book' 10th edition, Newnes-Butterworths, London 1973; Chapter 22, p. 497.

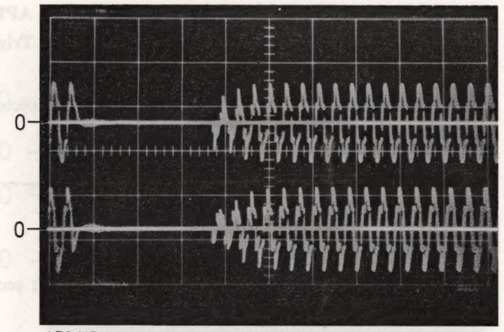

Fig. 15—Run-up of complete system:
currents flowing in two phases of transformer primary winding for initial V_c of 1·4V and final V_c of 3·0V
Vertical scale: 10A per main division
Horizontal scale: 50ms per main division

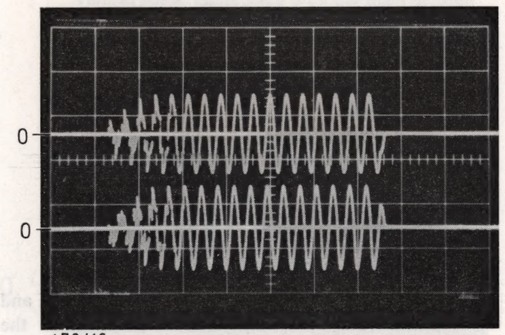

Fig. 16—Run-up of complete system:
currents flowing in two phases of transformer primary winding for initial V_c of 1·4V and final V_c of 3·5V
Vertical scale: 10A per main division
Horizontal scale: 50ms per main division

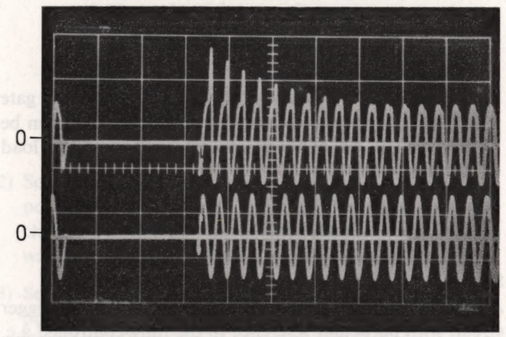

Fig. 17—Inrush current produced in one phase of transformer primary winding when run-up is too short
Vertical scale: 10A per main division
Horizontal scale: 50ms per main division

APPENDIX 1
Trigger Circuit

Component list

The following components are required for the complete trigger system.

Modules

3×RSA61
3×2NOR61
16×UPA61
3×TT61 (6×TT61 for larger gate drive; see Fig. 18)
3×mains transformers 17V output

Capacitors

1×2200μF 40V 071 17222
3×100μF 40V 016 17101
3×220nF C280AE/P220K
1×10nF C280AE/P10K
3×47pF

Resistors

3×10kΩ 10-turn potentiometer
3×50kΩ 10-turn potentiometer
1×470Ω CR25
3×2·7kΩ CR25
7×4·7kΩ CR25
3×6·8kΩ CR25
24×33kΩ CR25

NOTES

1) The components UPA61 module, 10nF capacitor, and the 470Ω and 4·7kΩ resistors are required in the positions marked † in Fig. 3b for a single trigger board only. These components perform the function of the master pulse train generator.
2) The TT61 trigger transformer can be conveniently mounted in the plastic chassis type UMC60. The trigger transformer configuration of Fig. 1 gives the following approximate extremities for the load line:

V_{GK}open-circuit = 8V,
I_{GK}short-circuit = 850mA.

When using higher-power thyristors with large gate drive requirements, the configuration of Fig. 18 can be used where the approximate extremities of the load line are:

V_{GK}open-circuit = 8V,
I_{GK}short-circuit = 1·7A.

Setting-up procedure for thyristor trigger circuit

A detailed setting-up procedure for the thyristor trigger circuit with particular reference to the fully-controlled a.c. controller is given here. The waveforms referred to can be identified from the block diagram, Fig. 2. The numbers in the blocks correspond to the printed-wiring board layout shown in Fig. 3b.

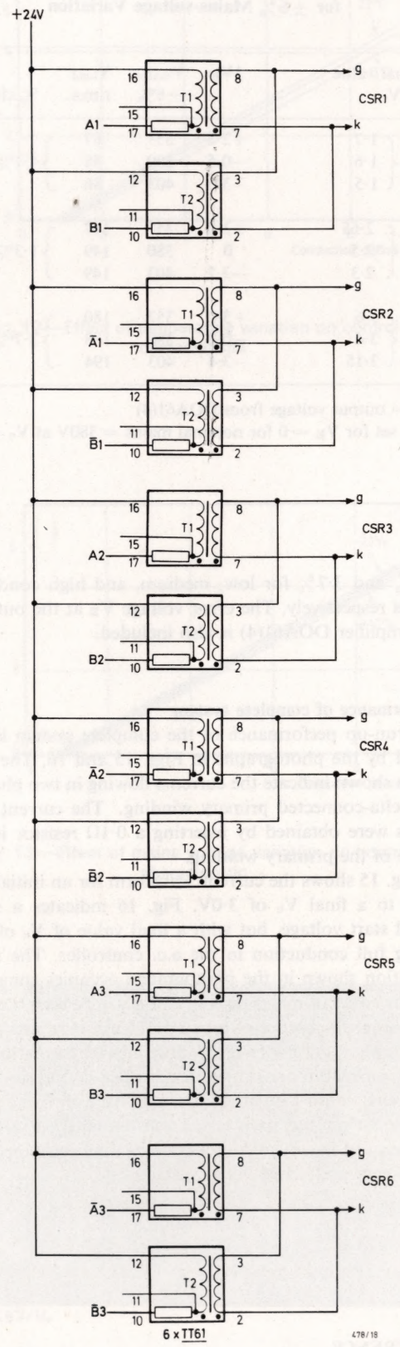

Fig. 18—Trigger transformer configuration for higher gate drive

Preliminary checks

1) Check the a.c. and d.c. power supplies.
2) Disconnect the V_c signal from the slow-start/voltage-compensation board, and connect an external supply variable from 0 to +5V with respect to the 0V line for the V_c control signal.
3) Using an extender board (MC60 03920) to make the circuit module pins accessible, the waveforms listed below should be checked. The waveform should correspond to that shown in the appropriate photograph. These checks ensure that the three trigger boards are functioning correctly.
   Synchronising waveform, block 6, pin 6: upper trace, Figs. 19 and 20
   Capacitor reset sync pulse, block 6, pin 8: middle trace, Fig. 19
   Ramp generator waveform, block 6, pin 15: lower trace, Fig. 19
   Q_1 timing waveform, block 5, pin 14: upper middle trace, Fig. 20
   Q_2 timing waveform, block 5, pin 5: lower middle trace, Fig. 20
   Bistable phase angle reset pulses, block 1, pin 11: bottom trace, Fig. 20
4) Check phase rotation of a.c. lines to transformers as shown in Fig. 1.

Setting-up procedure

1) Set the external V_c signal to some value between 0 and 5V, and observe the synchronising waveform at pin 6 of block 6, and the Q_1 timing waveform at pin 14 of block 5. The waveforms should have the form shown in Fig. 21.

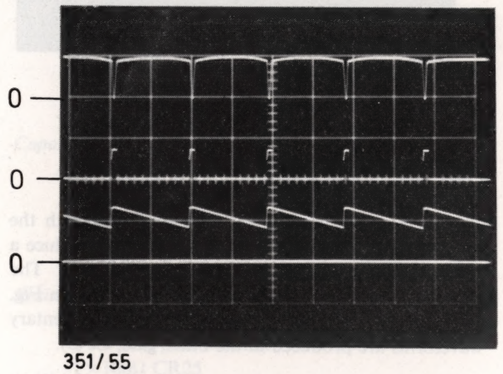

Fig. 19—Synchronising and ramp generator waveforms
upper: synchronising waveform
middle: capacitor reset synchronising pulses
lower: ramp generator waveform
Vertical scale: upper trace 0·5V per main division
middle trace 10V per main division
lower trace 5V per main division
Horizontal scale: 5ms per main division

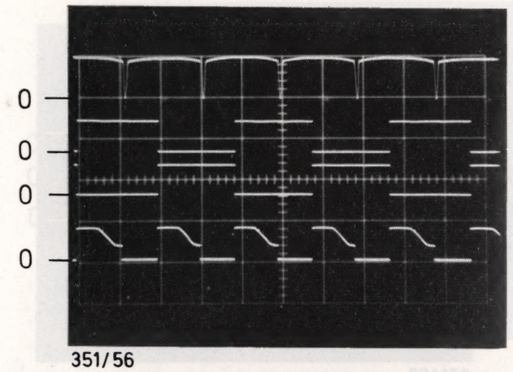

Fig. 20—Synchronising, Q_1 and Q_2, and pulse train timing waveforms
upper: synchronising waveform
upper middle: Q_1 timing waveform
lower middle: Q_2 timing waveform
bottom: bistable phase angle reset pulses
Vertical scale: upper trace 0·5V per main division
other traces 20V per main division
Horizontal scale: 5ms per main division

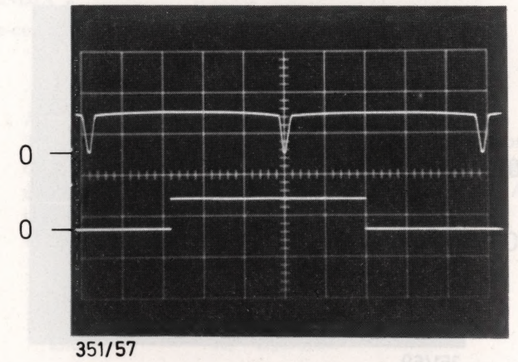

Fig. 21—Alignment waveforms for non-aligned board
upper: synchronising waveform
lower: Q_1 timing waveform
Vertical scale: upper trace 0·5V per main division
lower trace 20V per main division
Horizontal scale: 2ms per main division

2) Set the external V_c signal to 4·5V. Adjust the 50kΩ potentiometer P_2 so that the delay between the synchronising pulse and the positive edge of the Q_1 timing waveform is 1ms, as shown in waveforms of Fig. 22.
3) Set the external V_c signal to zero. Adjust the 10kΩ potentiometer P_1 so that the delay between the synchronising pulse and the positive edge of the Q_1 timing waveform is 8ms. (It is more convenient to observe the delay between the timing waveform and the next synchronising pulse which is (10—8) = 2ms, as shown in the waveform of Fig. 23.)

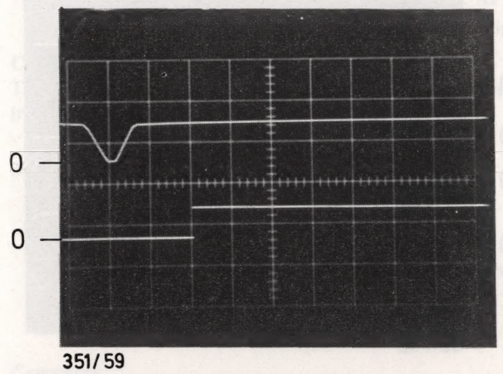

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Fig. 22—Waveforms in correctly-aligned board for 4·5V control signal
upper: synchronising waveform
lower: Q_1 timing waveform
phase delay between synchronising pulse and positive edge adjusted to 1ms
Vertical scale: upper trace 0·5 V per main division
lower trace 20V per main division
Horizontal scale: 0·5ms per main division

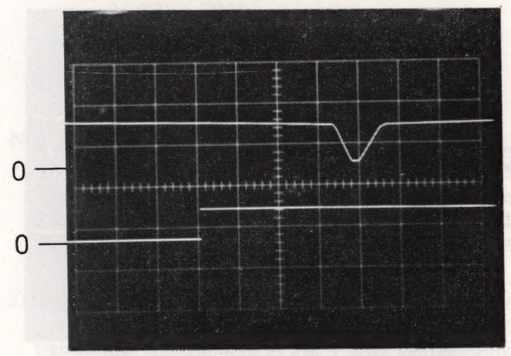

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Fig. 23—Waveforms in correctly-aligned board for 0V control signal
upper: synchronising waveform
lower: Q_1 timing waveform
phase delay between positive edge and synchronising pulse adjusted to 2ms
Vertical scale: upper trace 0·5V per main division
lower trace 20V per main division
Horizontal scale: 0·5ms per main division

4) Repeat steps 2 and 3 (as the potentiometers are interactive) until the board is correctly set up with delays of 1ms for V_c of 4·5V and 8ms for V_c of 0V.

5) Check the gating of the timing waveforms Q_1 and X_1 with the pulse train P. The waveforms associated with gate EF(4) are shown in Fig. 24, and are listed below.
Q_1 timing waveforms, block 5, pin 14: upper trace
X_1 timing waveform, edge connector: upper middle trace

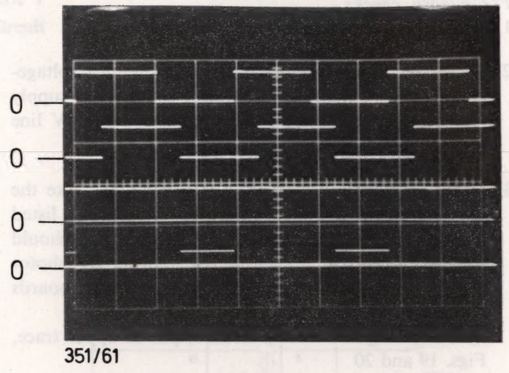

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Fig. 24—Production of 120° gated trigger pulse train
upper: Q_1 timing waveform
upper middle: X_1 timing waveform
lower middle: continuous pulse train P
bottom: gated pulse train
Vertical scale: 20V per main division
Horizontal scale: 5ms per main division

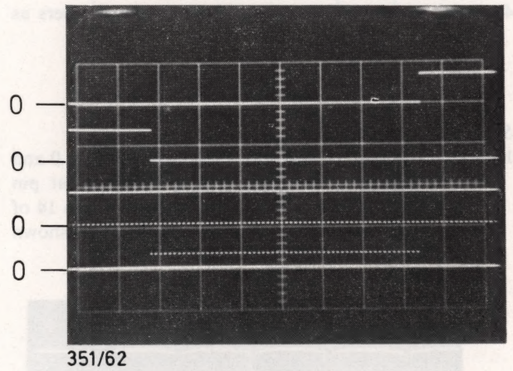

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Fig. 25—Expanded waveforms of Fig. 24
Horizontal scale: 1ms per main division

Pulse train P, edge connector: lower middle trace
Gated pulse train, block 4, pin 11: bottom trace
The timing waveforms Q_1 and X_1 are gated with the continuous trigger pulse train P in EF(4) to produce a trigger pulse train of 120° duration (6·6ms). The waveforms in Fig. 25 are an expansion of those in Fig. 24 to show the trigger pulses. The complementary waveforms are produced in the other gate, EF(3).

6) Check the outputs from the power amplifiers PA(1) to PA(4). The trigger pulse waveforms A and $\bar{A}$ for a V_c signal of 4·5V are shown in Fig. 26, and those for a V_c signal of 0V are shown in Fig. 27. Similar waveforms are associated with B and $\bar{B}$.

The setting-up procedure is now complete. The V_c signal from the slow-start and voltage-compensation board should be reconnected.

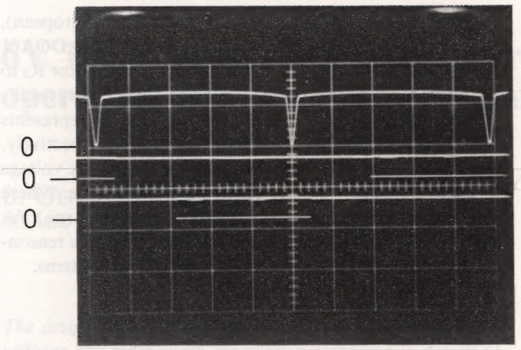

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Fig. 26—Pulse train waveforms A and $\bar{A}$ for 4·5V control signal
upper: sychronising waveform
middle: waveform A
lower: waveform $\bar{A}$
Vertical scale: upper trace 0·5V per main division
other traces 50V per main division
Horizontal scale: 2ms per main division

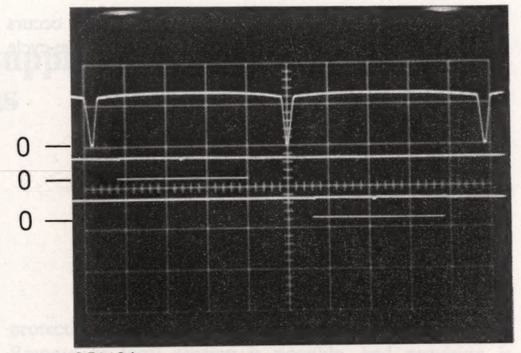

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Fig. 27—Pulse train waveforms A and $\bar{A}$ for 0V control signal
upper: synchronising waveform
middle: waveform A
lower: waveform $\bar{A}$
Vertical scale: upper trace 0·5V per main division
other traces 50V per main division
Horizontal scale: 2ms per main division

APPENDIX 2

Slow-start and Voltage-compensation Controller

Component list

The following components are required for the construction of the slow-start and voltage-compensation circuit.

Modules

4×DOA61

Diodes

7×BAX13
2×BZY88–C5V1
2×BZY88–C12

Capacitors

1×1000μF 40V 071 17102
2×3·3μF 100V 344 21335
1×68nF 344 21683
1×15nF C280AE/P15K

Resistors

1×1kΩ preset potentiometer
1×4·7kΩ potentiometer
1×100Ω CR25
2×330Ω CR25
3×1kΩ CR25
1×1·5kΩ CR25
2×3·9Ω CR25
4×47kΩ CR25
1×82kΩ CR25
2×100kΩ CR25

Alignment of slow-start and voltage-compensation circuit

The following alignment procedure (including the selection of run-up timing components) should be used for setting-up the slow-start and voltage-compensation circuit. A worked example is also given.

1) Set the value of V_{step} from:

$$V_{step} = \frac{R_2}{R_1+R_2} \times 5{\cdot}1 \text{ volts},$$

and: $R_1+R_2 \simeq 5k\Omega$.

The value of V_{step} for minimal transients can be experimentally determined by replacing R_1 and R_2 with a 5kΩ potentiometer. It has been found by experience that an empirical value for V_{step} of 1·4V is a very good compromise for most transformer systems.
Thus for V_{step} = 1·4V:

R_1 = 3·9kΩ,

R_2 = 1·5kΩ.

2) The run-up time from $V_c = V_{step}$ to full control is set by using the equation:

$$\frac{dV_c}{dt} = \frac{V_{step}+5{\cdot}1}{RC}.$$

Note that dV_c/dt and V_{step} are interactive, and it is suggested therefore the value of V_{step} is set before assigning the values of the integration time-constant. For trigger circuits aligned by the setting-up procedure

in Appendix 1, maximum output voltage control occurs at approximately $V_c = 3{\cdot}5V$. Thus for, say, a five-cycle run-up time from $V_{step} = 1{\cdot}4V$ to $V_c = 3{\cdot}5V$:

$$t = 100ms,$$

and:

$$\frac{3{\cdot}5-1{\cdot}4}{100\times10^{-3}} = \frac{1{\cdot}4+5{\cdot}1}{RC}.$$

Setting $R = 100k\Omega$:

$$C = 3{\cdot}3\mu F \text{ (to nearest preferred value).}$$

3) For nominal input mains 415V U.K. (380V European), adjust RV_2 for zero output voltage (pin 4) from DOA61 (4) with $V_c = 2{\cdot}5V$. Secondly, adjust fixed resistor R_3 to the voltage-compensation controller for the best results for settings of V_c of 1·6, 2·5, and 3·4V. This represents small, medium, and large conduction angles respectively. A $\pm6\%$ variation from nominal mains supply voltage using a Variac is used to check the performance. Where this technique is not suitable (for example, for large kVA installations), the value for R of 82kΩ will give a reasonably good compromise for the majority of systems.

APPENDIX 3

Recommendations for Specification of Power Transformers

There is quite often confusion concerning the requirements of a transformer for use with a.c. phase-control equipment such as described in this article. The following general points are given to indicate a few important factors. Detailed transformer design for phase-control application is well established.

1) When using three-phase transformers with phase control in the primary circuit, it is preferable to use a delta configuration as this allows a path for circulating harmonic currents.
2) A reasonable leakage inductance is useful for allowance of some d.c. component and coping with harmonic spikes. A C-core or transformer with tight magnetic coupling is not preferable.
3) Some derating of the maximum flux density of the iron is essential.
4) A fully-controlled a.c. controlier system is preferable as this produces symmetrical waveforms.
5) The use of a good symmetrically-balanced trigger circuit which is not prone to drift (that is, giving rise to d.c. currents which lead to transformer saturation) is recommended (such as the system described here).

6V 100A switched-mode power supply operating directly from the mains

B. GEORGE
Mullard Central Application Laboratory

UDC 621.311.62[621.376.5]

The design and operation of a switched-mode power supply utilising the pulse-width modulation technique is described. The circuit delivers up to 600W and operates directly from 240V a.c. mains without using a 50Hz mains transformer. The overall efficiency is approximately 60 to 65%, and is almost independent of the load. The circuit can be modified to operate from other input voltages, including 50V d.c.

INTRODUCTION

The advantages of the switched-mode technique compared with conventional series stabilisation in power supply design were outlined in Ref. 1. The savings in size, weight, and efficiency are quite considerable particularly at high output powers. In the past, these advantages could not be fully realised because a 50Hz mains transformer was still required to convert the a.c. mains input to a lower voltage suitable for existing h.f. power transistors. However, now that transistors are available which can handle several hundreds of volts at high repetition rates, it is possible to rectify the mains directly and thus eliminate the need for the 50Hz mains transformer. Some disadvantages also arise, however, because the mains transformer is no longer available for isolation, or to act as an h.f. filter (to reduce interference passing back into the mains), or as an a.c. impedance (required at turn-on).

The switched-mode power supply (SMPS) described in this article is designed to provide 6V at up to 100A for use in computer logic applications. It has overcurrent protection, and the output voltage is fully isolated. Remote or local sensing is possible, and provision is made for 'ramping-up' and 'ramping-down' the output voltage in response to an externally applied control signal. The same circuit, with some modification, can be made to operate from lower d.c. input voltages such as 50V d.c. This requires a reduction in the turns ratio of the h.f. output transformer and the use of suitable output transistors for the lower input voltages and higher currents.

The circuit described in this article represents some of the initial Mullard work in the SMPS field. Development is still continuing in all respects of SMPS technology, and further articles will be published in due course.

BASIC OPERATION

The SMPS described in this article uses the pulse-width modulation method of control. This is a fixed-frequency system in which the conduction time of each output transistor is varied to change the amount of energy transferred to the load during each cycle.

The operation of the supply is shown schematically in Fig. 1. The mains input voltage is filtered, rectified, and smoothed to give approximately 280V d.c. The filter also reduces the noise, caused by high-speed switching edges, that is transmitted back into the mains. The d.c. voltage is then applied, via the primary of a ferrite-cored transformer, to push-pull switching transistors operating at a frequency between 20 and 25kHz. The voltage on the secondary of this transformer is rectified

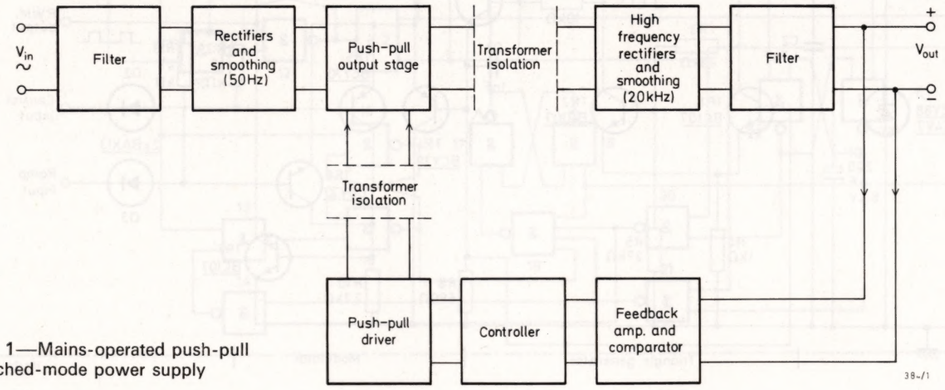


Fig. 1—Mains-operated push-pull switched-mode power supply

by high-current fast-switching diodes, and smoothed by a choke input filter to give the required d.c. output. A further filter may be added to reduce the level of generated noise reaching the output terminals.

The output voltage is monitored, either locally or remotely, and compared with a reference voltage. Any error signal is passed via an amplifier to the input of the SMPS controller. The controller converts the analogue error signal to a variable pulse-width signal and also directs alternate pulses to each side of the push-pull driver stage. The push-pull driver stage amplifies the pulse current to a level sufficient to drive the switching transistors. By varying the pulse-width, the amount of energy transferred to the load during each cycle can be controlled. In this way, stabilisation of the output voltage is achieved, the stability being dependent on the gain in the feedback loop.

The output is isolated from the input by the high-frequency (25kHz) output transformer and by the base-drive transformers of the switching transistors. Transformer base-drive allows all drive and feedback circuits to be directly coupled to each other and to the output, thus avoiding problems associated with a.c. coupling of the feedback circuits. The output voltage can be floated above or below earth potential, the limit being defined by the isolation resistance of the transformers.

A separate supply voltage is required to operate the various parts of the drive circuit. This can be obtained either from a small 50Hz mains transformer or from a separate switched-mode power supply running from the 280V supply. This is covered more fully later (page 116).

CONTROLLER

For a constant-frequency system under varying load and input voltage conditions, the output voltage is maintained constant by varying the transistor conduction time, or pulse width. By increasing the pulse width from zero to 100% of the switching period, the output voltage can be varied from zero to maximum, the upper limit being dependent upon the load and input voltage. The circuit which generates a constant frequency and converts the analogue signal from the feedback amplifier to a variable pulse-width switching waveform is shown in Fig. 2. Although this circuit is fully described in Ref. 1, a brief outline of its operation is given below.

The Schmitt trigger, TR_1 and TR_2, and the integrator, TR_3 and C_3, together form a self-oscillating triangular waveform generator. The frequency of the waveform is set by the value of C_3. The waveform is applied to one input of a long-tailed pair, TR_4 and TR_5, while a control signal from the feedback amplifier is applied to the other input. By varying the d.c. level of the control signal, the trip point of the long-tailed pair is altered, and hence the width of the pulse at the collector of TR_7 is varied. Transistor TR_6 in parallel with TR_5 provides for override functions such as ramp-up at turn-on.

In a push-pull SMPS, the variable pulse-width signal is applied alternately to the two output switching transistors. This is achieved using the circuit shown in Fig. 3.

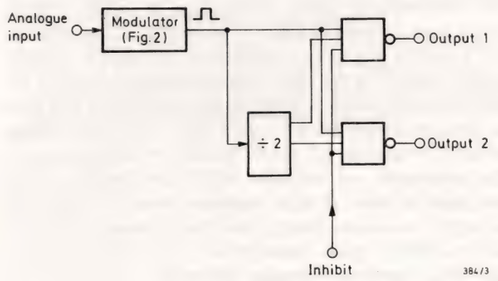


Fig. 3—Pulse gating circuit

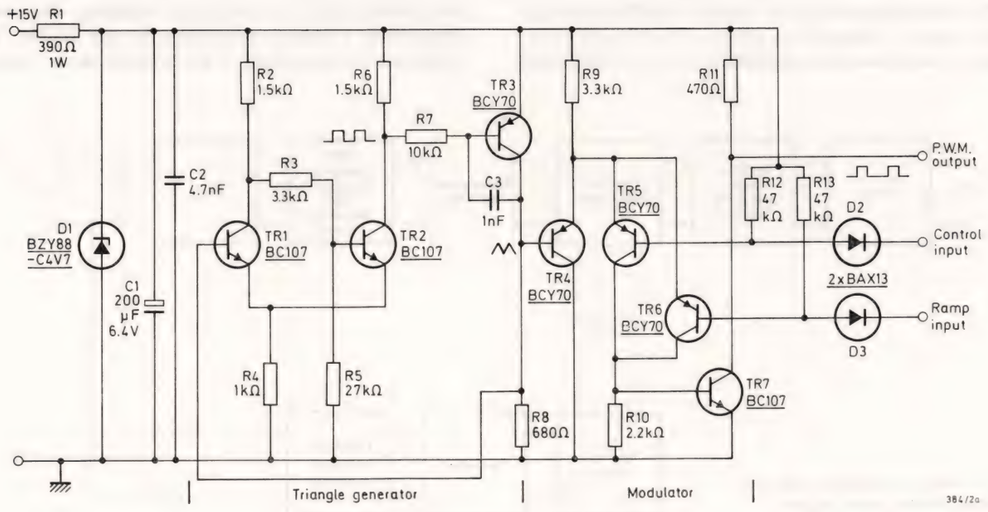


Fig. 2—Variable pulse-width generator

The falling edge of each pulse leaving the modulator is used to trigger a divide-by-two circuit. The complementary outputs of the divide-by-two circuit are used to gate each pulse to alternate output transistors. The inhibit input can be used to prevent turn-on of the transistors during overload or fault conditions, even though the feedback signal to the controller requests a wider pulse width.

The complete circuit of the SMPS controller is shown in Fig. 4. Gates 6 and 7 gate alternate pulses to the appropriate output pin, P_1 or P_2, determined by the divide-by-two circuit and the pulse from gate 5, as described above. Gates 6 and 7 also prevent the pulses generated in the modulator from reaching the outputs during an inhibit condition. When an inhibit condition occurs, the inhibit input I goes LOW and gates 17, 18, and 19 switch over, clamping the output of gate 17 LOW. After removal of the inhibit condition, the output of gate 17 will remain LOW until two conditions are satisfied. Firstly, the next output to conduct after an inhibit must not be the same as the output conducting immediately prior to shutdown. If this is not so, one output could conduct on several successive pulses, and this could lead to excessive magnetising current in the output or drive transformers, which could damage the output switching transistors. (This condition is monitored by gates 20 to 23.) Secondly, the output must not resume while a pulse is being generated by the modulator, otherwise the very end of a pulse may be sufficient to trigger the control logic but not long enough to turn on the output switching transistor. (This is performed by gates 13 to 16.) The remaining gates are required for internal organisation of the control logic. If a 50/50 mark-to-space ratio were used such that the drive to one output switching transistor turned on immediately the other one turned off, problems could arise due to the turn-off time being longer than the turn-on time. In such a case, both transistors could conduct simultaneously, resulting in a virtual short-circuit across the supply voltage. To prevent this from occurring, a minimum dead time or maximum pulse width is defined. As the optimum dead time varies for different output switching transistors and even for different methods of driving one transistor, it is necessary that this parameter should be variable. This is achieved by inhibiting the variable pulse at gate 1 for a time defined by the monostable timing capacitor and resistor, C_{mp} and R_{mp} respectively.

The entire circuit of Fig. 4 can be built using discrete

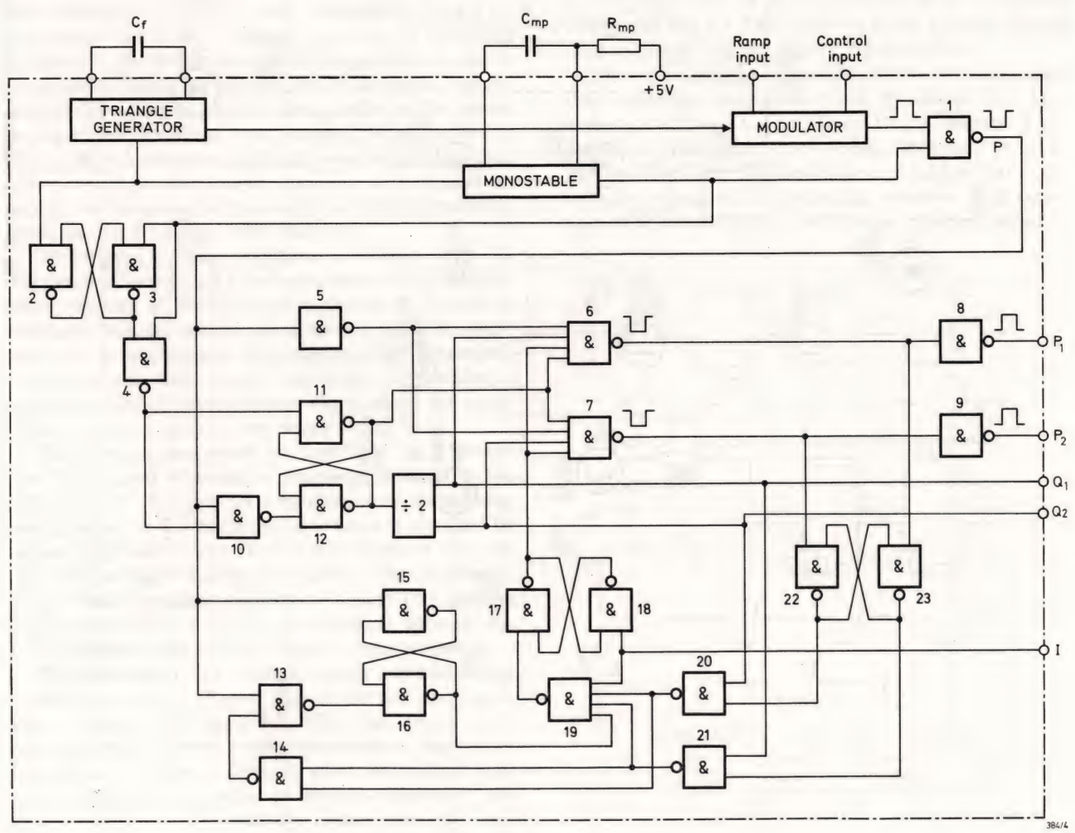


Fig. 4—Complete SMPS controller

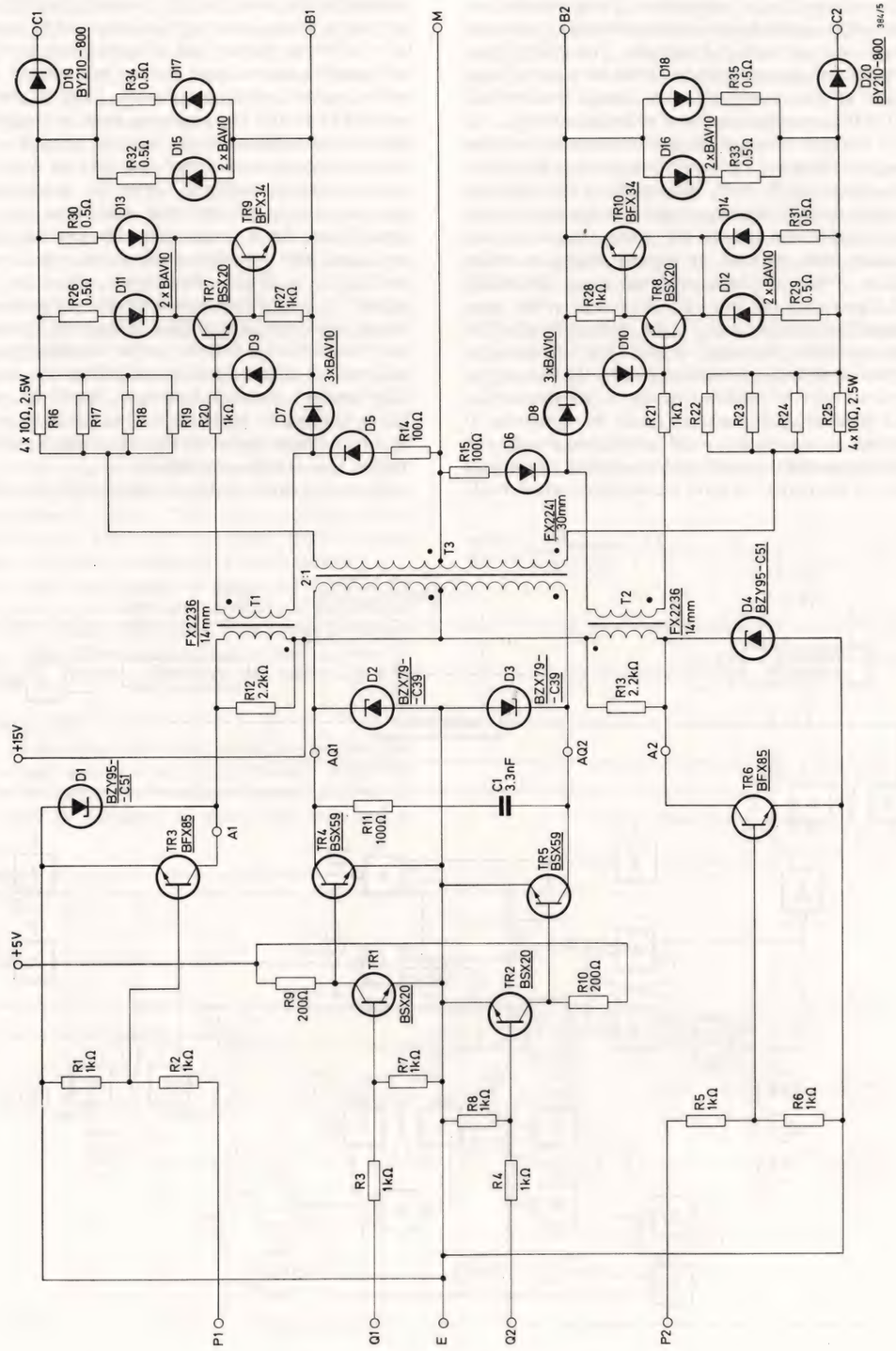


Fig. 5—A.C. coupled push-pull driver

components and logic gates; alternatively it is suitable for integration (the dotted line indicates the external connections). A more versatile circuit using integrated circuit techniques is at present being developed.

PUSH-PULL DRIVER

A driver circuit is required to convert the current level at the output of the controller to that required to drive the output switching transistors. The driver stage is shown in Fig. 5. This circuit is a.c. coupled to the output switching transistors to isolate the feedback circuit from the output.

Transformer coupling is the most convenient method for achieving isolation up to several kilovolts. However, there are difficulties in designing transformers to operate with widely varying pulse widths. These arise primarily from the necessity to derive both turn-on and turn-off drive currents from one transformer. In a given application, the energy required for one of these operations is derived from the stored magnetising energy in the transformer core. As this stored energy is a function of conduction time, a variation in drive conditions at different pulse widths results.

The drive circuit shown in Fig. 5 attempts to overcome this difficulty by utilising two transformers: one (T_3) to provide the power required to drive the switching transistors, this power being provided for the full period of possible conduction of each output transistor, and the second (T_1 or T_2) to gate the drive current to the appropriate output transistor when required. In other words, T_3 is a 50/50 mark-space push-pull transformer, providing drive current to each output transistor in turn, and T_1 and T_2 are low-power single-ended transformers operating from zero to 50% pulse-width (variable).

Magnetising current problems associated with T_3 are minimal because it is a push-pull transformer. Furthermore, because of the push-pull action in T_3, it can be arranged that the positive drive current to each output transistor is accompanied by a negative (that is, turn-off) current to the other output transistor, so providing a controlled turn-off characteristic. Fig. 6 shows the waveforms at various points in the circuit of Fig. 5.

The damping components R_{11} and C_1 in Fig. 5 prevent the development of excessive overswing voltages at the collectors of TR_4 and TR_5 by dissipating magnetising energy stored in T_3. Additional protection is provided by voltage regulator diodes D_2 and D_3. Resistors R_{12} and R_{13} dissipate stored energy in T_1 and T_2 after each cycle. Buffer stages comprising transistors TR_1 and TR_2, running from a separate 5V supply, are inserted between the drive transistors TR_4 and TR_5 and the inputs Q_1 and Q_2.

The secondary of T_3 is connected via current-limiting resistors R_{16} to R_{19} (R_{22} to R_{25}) to the two Darlington drive transistors TR_7 and TR_9 (TR_8 and TR_{10}) which act as emitter followers in the base leads of the output transistors. As shown in Fig. 6, when one output transistor turns off, for example at the end of pulse P_1, the drive transformer T_3, which is driven from Q_1, also switches and provides negative drive to hasten switch-off. It also provides drive to turn the other output transistor on when required, at the beginning of pulse P_2. When this occurs, the current from T_3 is gated into this output transistor and will remain until both P_2 and Q_2 go negative together, so repeating the cycle. During the transition, it is important that the gating pulse should not be removed before the drive current has reversed, otherwise the output transistor will effectively be left with an open-circuit base and no turn-off current. However, in the present circuit, the delay between the generation of the gating pulse and the drive pulse is negligible compared with the turn-off time of the output transistors.

The negative drive is provided by the conduction of diodes D_{15} and D_{17} (D_{16} and D_{18}), and here care must be taken not to exceed the reverse V_{BE} rating of the output transistor. At the instant of turn-off, the reverse voltage applied to terminal B_1 is limited by the voltage drop across R_{16} to R_{19} while reverse base current flows. When all stored charge has been removed from the base, the voltage across R_{16} to R_{19} falls to zero and a greater reverse voltage occurs across the base-emitter junction of the output transistor. The maximum reverse voltage $V_R$max occurring at the base-emitter junction is thus:

$$V_R\text{max} = [\{V_s — V_{CE}(\text{driver})\} \times (N_2/N_1)] — V_D, \quad \ldots (1)$$

where V_s is the supply voltage to T_3, N_1/N_2 is the transformer turns ratio of T_3, V_{CE} (driver) is the bottoming voltage of TR_4 (or TR_5), and V_D is the forward voltage drop of diodes D_{15} and D_{17} (or D_{16} and D_{18}).

The output transistors are held out of saturation during their respective conduction times by diodes D_{11}, D_{13}, and D_{19} (or D_{12}, D_{14}, and D_{20}). This is essential if the maximum conduction time of each transistor is to be accurately defined. The diodes are arranged so that as the collector voltage of the conducting transistor falls, excess base drive current is bypassed into the collector instead of

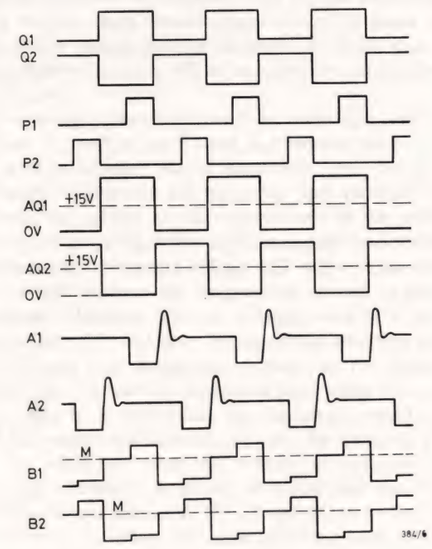


Fig. 6—Waveforms associated with driver

the base before excessive base-storage occurs. In this way, the collector-emitter/voltage of the transistor is defined as:

$$V_{CE}(\text{output}) = V_{BE}(\text{output}) + V_{BE}(TR_9) + V_{CE}(TR_7) + + V_D(D_{11}) - V_D(D_{19}). \quad \ldots(2)$$

Thus, if $V_D(D_{19}) \simeq V_D(D_{11})$,

$$V_{CE}(\text{output}) \simeq V_{BE}(\text{output}) + V_{BE}(TR_9) + V_{CE}(TR_7).$$

The output transistors in this power supply are type BDY96-01. Because of the high-voltage capability of this device, the collector-emitter saturation voltage is also relatively high. Thus the value of V_{CE}(output) in Eq. 2. is nominally 1·7V.

It should be noted that diodes D_{19} and D_{20} are capable of withstanding the same maximum voltage as the output transistors; that is 800V. They must also have a reasonably fast switching speed (<300ns) to prevent diode storage time from affecting the turn-off characteristic of the output transistor.

PUSH-PULL SWITCHING STAGE

The basic components of the push-pull switching stage are shown in Fig. 7. The output transformer T_2 converts the high voltage at its primary to the required output voltage, in this case 6V. Diodes D_3 and D_4 are high-frequency rectifiers and are required to have the lowest possible forward voltage drop at the required output current, since a 1V drop in the rectifiers is equivalent to almost 20% loss in efficiency. Schottky-barrier rectifiers are therefore preferred because their forward voltage drop is approximately half that of diffused silicon rectifiers. Also, these rectifiers can be used up to 1MHz which is not possible with silicon diffused rectifiers at high output currents. However, their reverse voltage ratings are often limited and therefore safety margins for component tolerances must be considered carefully. The use of several diffused junction rectifiers in parallel is a possible alternative, but the additional forward voltage drop, including that across the current-sharing resistors, would again result in a reduction in overall efficiency of between 10 and 20%.

The output filter, L_1 and C_5, is required to attenuate the switching-frequency ripple voltage to an acceptable level, thus producing a d.c. output voltage. A ripple voltage at the switching frequency is inherently superimposed on the d.c. output voltage, but this can be kept small by correct choice of components. A compromise must be made, however, because the output filter is within the feedback loop, and excessively high filter component values can cause instability.

Operation

The operation of the output stage (Fig. 7) is as follows. As each transistor conducts in turn, the voltage developed across each half of the secondary of T_2 is given by:

$$V_2(T_2) = [V_s - V_{CE}(TR_1) - V_1(T_1)]\ N, \quad \ldots(3)$$

where V_s is the d.c. supply voltage, $V_{CE}(TR_1)$ is the voltage dropped across the conducting transistor, $V_1(T_1)$ is the voltage dropped across the primary of the current-monitoring transformer T_1, and N is the turns ratio of T_2. As T_1 is a current transformer with a high turns ratio (70:1, see Appendix 4), $V_1(T_1)$ is small compared with the supply voltage. The bottoming voltage $V_{CE}(TR_1)$ of the output transistor is also small. Thus, almost the total supply voltage appears across the primary winding of T_2.

As one output transistor conducts, say TR_1, rectifier

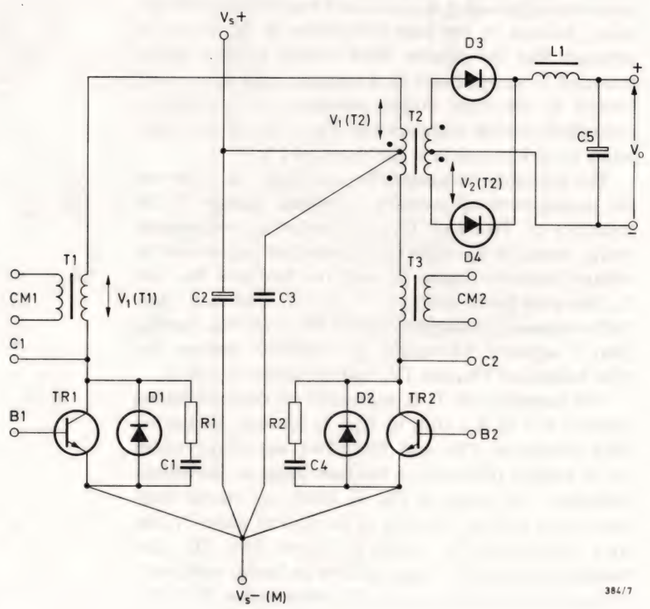


Fig. 7—Push-pull output switching stage

D_3 will also conduct. For a secondary voltage $V_2(T_2)$ and an output voltage V_o, the voltage appearing across the filter inductance is:

$$V(L_1) = V_2(T_2) - V_o - V(D_3), \quad \ldots(3)$$

and the current through the inductor L_1 rises at the rate $(di/dt)_r$ given by:

$$\left(\frac{di}{dt}\right)_r = \frac{V(L_1)}{L} = \frac{V_2(T_2) - V_o - V(D_3)}{L}, \quad \ldots(4)$$

where $V(L_1)$ is the voltage across L_1, L is the inductance of L_1, and where $V(D_3)$ is the voltage drop across the rectifier D_3. When TR_1 ceases to conduct, there is a dead time before TR_2 commences conduction. During this time, the current through the inductor attempts to continue to flow by generating a back e.m.f. which causes the cathode of D_3 to go negative until both D_3 and D_4 conduct. Each diode then carries half the inductor current. The reverse voltage across L_1 now causes the inductor current to fall at the rate $(di/dt)_f$ given by:

$$\left(\frac{di}{dt}\right)_f = -\frac{V_2(T_2) + V_o + V(D_3)}{L}, \quad \ldots(5)$$

where $V_2(T_2)$ is now zero.

As $V_2(T_2)$, V_o, $V(D_3)$, and L are all constant for a given operating condition, the rates of rise and fall of current are also constant. (In other words, the current rises and falls linearly.) Thus, a triangular current waveform is obtained, as shown in Fig. 8, the average current being equal to the d.c. load current.

When the inductor current is greater than the load current, the excess current passes into the filter capacitance (C_5 in Fig. 7), and when the inductor current is less than the load current, the extra current will be supplied by the filter capacitor. This gives rise to a ripple voltage on the filter capacitor.

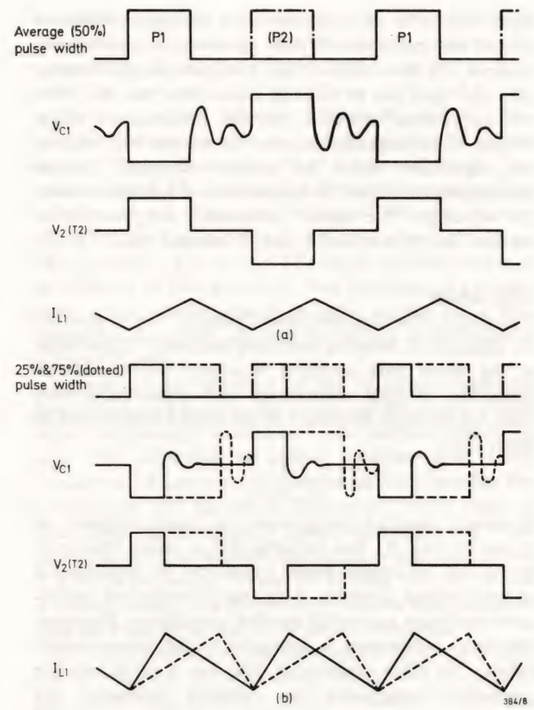


Fig. 8—Waveforms associated with output switching stage

Because of leakage inductance between the primary and secondary windings of the output transformer, a voltage spike is generated on the primary whenever one of the output transistors is turned off. This adds to the effect of the primary magnetising current, and the resulting voltage spike may be dangerous in two ways: firstly, an excessive overswing voltage may exceed the V_{CEO}max rating, or even the V_{CBO}max rating, of the output transistor, and secondly an overswing voltage of greater than the supply voltage (that is, V_{CE} during overswing $>2V_s$) will cause the collector of the opposite output transistor to go negative with respect to the emitter. If this negative voltage exceeds the reverse V_{BE} rating of the device plus one diode forward voltage drop (that is, about 6·7V), the collector-base diode will conduct and also the base-emitter diode will be reverse-biased beyond its breakdown voltage. This will lead to high emitter-base current and probably result in the destruction of the device.

There are two possible precautions. To prevent the overswing voltage from exceeding the supply voltage, a diode (D_1 or D_2) is connected between the collector and emitter of the output transistor, as shown in Fig. 7. This diode is normally reverse-biased, but when the collector goes negative it will conduct and clamp the voltage at only −0·7V. The diode must be able to withstand the full collector voltage (that is, $>2V_s$), and also operate faster than the output transistor to prevent a further negative transient. If necessary this can be achieved by using two or more lower-voltage diodes in series with appropriate voltage-sharing resistors, in which case the total negative transient will be increased by the number of diodes used.

Overswing is also minimised by inserting a damping network (C_1 and R_1, or C_4 and R_2) between the collector and emitter of each output transistor. This damps the overswing voltage to less than V_s, and therefore also prevents the voltage at the opposite end of the primary of T_2 from dropping below earth. It should be noted that the maximum overswing voltage will occur at maximum pulse width because the magnetising current is then a maximum. However, whereas a large value of C and a small value of R will have the maximum damping effect, the charging and discharging currents in the capacitor will be high. Conversely, although a small value of C and a large value of R will reduce the discharge current spike into the output transistor at turn-on, the damping effect will be minimised. For this reason, a compromise is obviously necessary. It should be noted that the values of these components must be chosen so as to maintain the transistors within their safe operating area (SOAR) curves (Ref. 2).

Once the correct choice of damping component has

been made, the primary-secondary leakage inductance should not cause any further problems. An imbalance between the two primary (or two secondary) windings may also give rise to leakage inductance, but this effect will be minimal provided that the windings are bifilar wound. This particular leakage inductance will be even less significant when the primary-secondary leakage inductance is increased by the insertion of a screen between the windings. The screen is essential for interference reasons, and is discussed in Ref. 3 (see also page 116).

Filter design

The output filter requires careful design if it is to perform its function of reducing switching-frequency ripple while at the same time avoiding secondary effects such as instability. If ideal inductances and capacitances were used, the resonant frequency of the output filter would be given by:

$$f_o = \frac{1}{2\pi\sqrt{(LC)}}.$$

However, practical components are more complex, as shown in Fig. 9. The inductor has a series resistance, giving rise to copper losses which can be considerable at high output currents. Also, the interwinding capacitance produces an overall parallel capacitance. However, this latter component is negligible in the present application. The filter capacitance also has a series resistive component comprising the dielectric resistance, the resistance of the electrolyte, and that of the connecting leads. There is an inductive component, and also a parallel resistance derived from the insulation resistance within the capacitor.

Of all these, the series resistance of each component and the inductance of the capacitor are the most important. They can give rise to losses in addition to affecting the resonant frequency of the filter.

The requirements of the filter inductor are as follows:

1) Adequate inductance to attenuate the switching-frequency ripple voltage by the desired amount;
2) Minimum series resistance to limit dissipation;
3) The ferrite core material must not saturate under the influence of large d.c. components of current (that is, a large air gap will be necessary).

For the present application an inductance of 6·5μH is required, carrying a maximum current of 130A.

The requirements of the filter capacitor are:

1) Adequate capacitance to attenuate the switching-frequency ripple voltage by the desired amount;
2) Minimum series resistance to limit dissipation and to prevent additional ripple voltages being generated. (A series resistance of 10mΩ with 10A flowing through the capacitor will give rise to an additional 100mV peak-to-peak ripple voltage.)
3) Minimum series inductance to limit additional ripple voltage, and also to provide maximum possible attenuation.

Fig. 10 shows the effective circuit of the output filter including all the critical parasitic components. For the

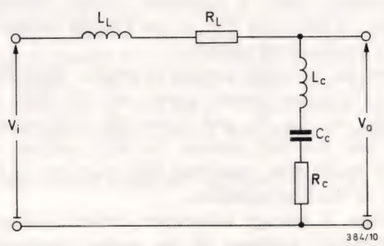


Fig. 10—Effective output filter impedances

present application, a 106 series capacitor was chosen because of its low series inductance and resistance (Refs. 4 and 5). Its value is 100 000μF, 10V (type 106 14104). The resonant frequency of the output filter is thus:

$$f_o = \frac{1}{2\pi\sqrt{(LC)}} = \frac{1}{2\pi\sqrt{(6{\cdot}5\times10^{-6}\times0{\cdot}1)}},$$

$$= 197{\cdot}4\text{Hz}.$$

However, the effect of the series inductance of the capacitor is to prevent the total loop phase shift from reaching 360° until a higher frequency.

Heatsink requirements

In the worst-case, it can be calculated that the total dissipation in both output transistors is 15·7W, (see Appendix 1). Therefore, if a maximum ambient temperature of 70°C within the unit is specified, the maximum junction temperature is 125°C. The thermal resistance of the required heatsink is given by:

$$R_{th(h-a)} = R_{th(j-a)} - R_{th(j-mb)} - R_{th(mb-h)}, \quad ..(8)$$

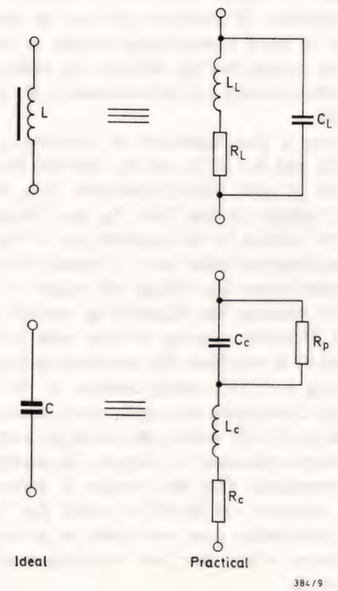


Fig. 9— Ideal and practical output filter inductor and capacitor

where $R_{th(j-a)}$ is the thermal resistance between junction and ambient, $R_{th(j-mb)}$ is the thermal resistance from junction to mounting base, and $R_{th(mb-h)}$ is the thermal resistance from mounting base to heatsink. Therefore,

$$R_{th(h-a)} = \frac{(125-70)}{15{\cdot}7} - 1{\cdot}5 - 0{\cdot}3,$$

$$= 1{\cdot}7\text{degC/W}.$$

A similar procedure is used to calculate the heatsink requirements for the high-frequency output rectifiers.

FEEDBACK AMPLIFIER

The main requirements of the feedback amplifier are as follows:

1) Appropriate loop gain/phase characteristic to give stability with local or remote sensing;
2) A high d.c. gain for good load and line regulation;
3) A high loop gain at 100Hz for effective reduction of mains-frequency ripple;
4) Adequate loop gain at medium frequencies to provide a reasonable transient response;
5) High rejection of frequencies above about 20kHz to prevent switching-frequency ripple causing instability.

These requirements to some extent conflict so a compromise is obviously necessary. The basic problems of feedback design are primarily the same as those associated with conventional power supplies except for two factors. Firstly, the output LC filter is within the feedback loop, and as the component values are relatively high, the resonant frequency is relatively low (as described earlier). Secondly, there is an inherent switching-frequency ripple voltage at the output which would result in oscillation if the gain were greater than unity at the switching frequency.

The circuit of the feedback amplifier is shown in Fig. 11. The output voltage of the power supply is fed back to the input of the feedback amplifier, at the base of TR_1, and compared with a fraction of the reference voltage at the base of TR_2. The circuit shown uses discrete components but an integrated operational amplifier, for example TBA221, could be used.

Fig. 12a shows where the fundamental gain and phase shift components occur within the loop, and Fig. 12b shows a typical loop frequency response. The double roll-off is caused by the inductance of the filter capacitor which prevents the phase shift from approaching the −360° condition until the feedback amplifier takes over.

PROTECTION CIRCUIT

The power supply includes overcurrent protection which prevents it from supplying excessive current and damaging both itself and the load if the latter develops a fault. The method of sensing excessive current is shown in Fig. 13. Two small transformers T_1 and T_3 are placed in series with the collectors of the two output transistors. The voltages developed across the primaries of these transformers can be made very small so that the operation of the power supply is not affected. A high turns ratio is used (70:1) to develop a higher voltage across resistors R_3 and R_4 connected to the secondary windings. Damping resistors (R_1 and R_2) are also required to dissipate the stored energy in the transformer cores at the end of each cycle. The currents in the secondaries of T_1 and T_3 are rectified and passed through resistors R_3 and R_4. The voltages developed across R_3 and R_4 are applied to the base of TR_3 which is the input of a long-tailed pair. The base voltage of TR_5 is set to give the maximum permissible collector current. If the base voltage of TR_3 ever exceeds this value, the long-tailed pair switches over, turning on TR_3. This turns TR_4 on and TR_5 off, so that the output at the collector of TR_7 goes high. This then triggers a monostable which inhibits the pulse-width output for a predetermined time, thus allowing the current in the inductor to decay to zero.

Because of the operation of the transformer-coupled drive circuit, it is not possible to turn off the control pulses unless the divide-by-two network also switches over at the same time, otherwise the output transistor base is left open-circuit. Therefore, it is most convenient to delay the inhibit pulse until the end of the present output pulse, at which time the transistor is turned off safely. This overcomes the problem of imbalance in the output transformer (T_2), while the output choke, by limiting the rate of rise of output current to a defined level, ensures that this delay does not result in substantially greater overloads.

At the end of the monostable inhibit time, the inhibit will be removed and the power supply will attempt to deliver an output. However, if the overload still exists, the system will shut down again, and then continue to try to deliver power repeatedly until the overload is removed. After an inhibit condition, the system will ramp-up slowly to avoid surge currents, just as it does at initial turn-on. This involves gradually increasing the ramp-up voltage input (see Fig. 2) so that the pulse duration gradually increases. If this were not done, the feedback amplifier would immediately ask for full output at turn-on, and the peak currents would retrigger the overload protection circuit to initiate shut-down.

By utilising a transformer-coupled current sensing circuit, the isolation of the mains-to-output voltage can be maintained, and the current sensing circuit can be directly connected to the system earth or common line. A single current-sense transformer in the combined emitter lead of the output transistors was considered, but the problems caused by the continuous d.c. current passing through the primary of the transformer make this solution economically impracticable. The current-sense transformers, like the output transformer, require screens for r.f.i. suppression (see page 116 and Appendix 4).

The other form of protection which has not yet been discussed is overvoltage protection. This is primarily designed to protect the load in the event of a fault in the power supply causing the output voltage to rise. This can sometimes occur in remote sensing operation if one of the sense connections is inadvertently disconnected. The feedback amplifier will then indicate a low output voltage, and the system will proceed to deliver more and more power. If the load current is low this increase in power will be experienced as an increase in output voltage and, provided that the total power supplied is within the capability of

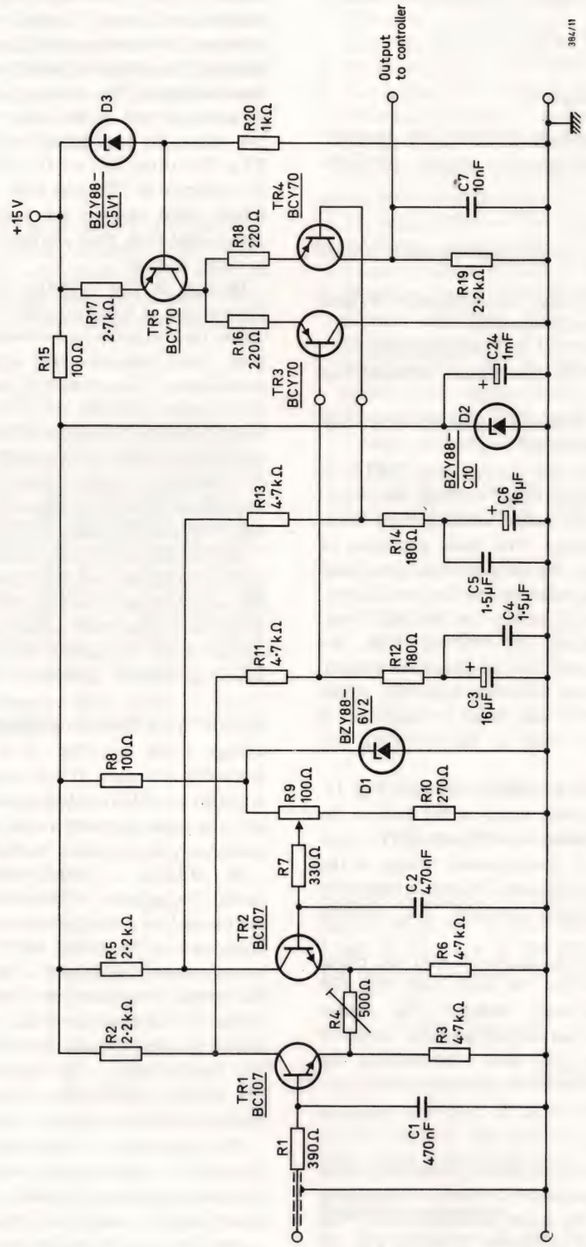


Fig. 11—Feedback amplifier

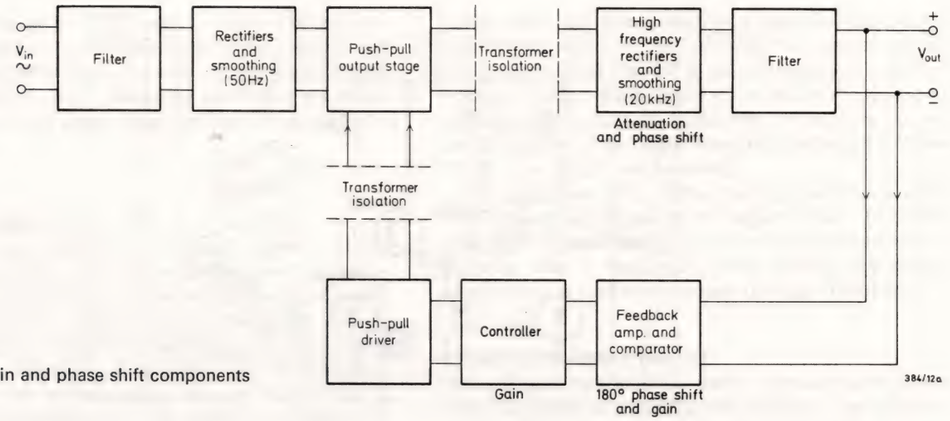
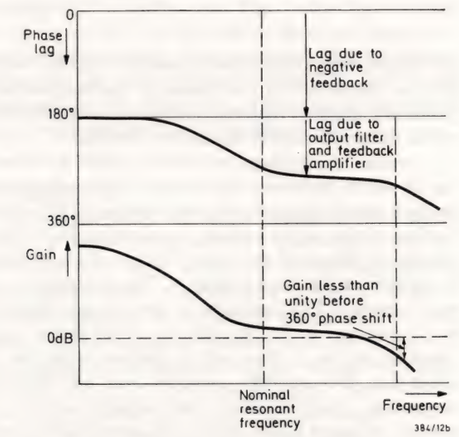


Fig. 12a—Gain and phase shift components

Fig. 12b—Typical loop frequency response



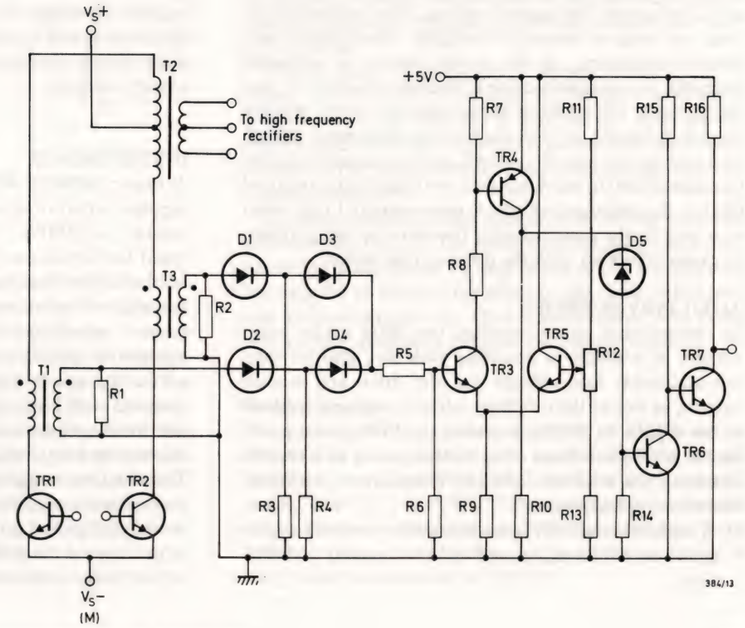


Fig. 13—Overcurrent protection circuit

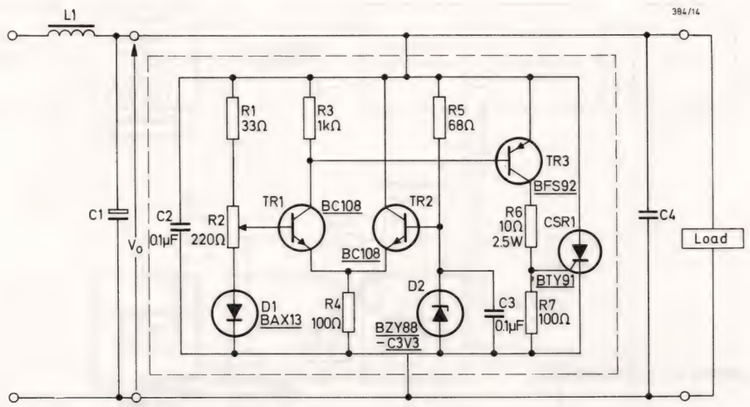


Fig. 14—Overvoltage protection circuit

the supply, the overcurrent protection circuit will not become operative. For this reason a separate overvoltage protection circuit is required, and this is best situated not within the power supply but near to the load.

A typical overvoltage protection circuit is shown in Fig. 14, and its operation is as follows. As the voltage across the load rises from zero, the base voltage of TR_1, being a fraction of the output voltage, remains less than the base voltage of TR_2 until the zener voltage of D_2 is reached. From then on, the base voltage of TR_2 is clamped and the base voltage of TR_1 continues to rise at a rate determined by the ratio set by R_1, R_2, and D_1. If the output voltage continues to rise, a point will be reached when the long-tailed pair, TR_1 and TR_2, switches over, and TR_3 begins to conduct. This transistor then supplies current to the gate of thyristor CSR_1 which will immediately conduct and short-circuit the output voltage, thus protecting the load. As long as current is available, the thyristor will remain conducting. If the power supply is operating correctly, the secondary current through the choke L_1 and the thyristor will continue to rise until an excess primary current is sensed by the overcurrent protection circuit. The system will then shut down, and continually attempt (unsuccessfully) to provide power, until the fault is removed (that is, the disconnected wire is reconnected). In the event of a fault in the power supply, the thyristor will continue to protect the load until the primary fuse blows.

AUXILIARY SUPPLIES

In conventional power supplies, the 50Hz mains transformer, in addition to providing isolation, also provides the additional low voltages for the drive and control circuits, as well as the stabilised reference voltages required in the supply. In SMPS, however, the 50Hz mains transformer is eliminated and other methods must be found for obtaining the auxiliary voltages. There are a number of alternative techniques.

1) A separate small 50Hz mains transformer with appropriate rectification, smoothing, and possibly stabilisation.
2) A dropper resistor from the 280V d.c. line
3) Further secondary windings on the high-frequency output transformer.
4) A separate high-frequency inverter running from the 280V d.c. line.
5) A separate small switched-mode power supply running from the 280V d.c. line.

Method 2 is not feasible in practice because of excessive dissipation in the dropper resistor and the lack of isolation. Method 3 is also not feasible if certain facilities, such as overload control circuits, are required to operate during an overload, when the output from the supply is zero. Method 4 is a practicable possibility and would provide a relatively small and cheap supply but with unstabilised voltages. The fifth method is the most sophisticated and potentially the most compact technique. However, it requires the design of a separate SMPS and therefore, in the power supply described in this article, method 1 is used, as the design is relatively simple and compact for the low powers required.

INTERFERENCE

A major problem when designing switched-mode power supplies is that of eliminating interference both inside and outside the SMPS. Radiation or transmission of high-speed low-impedance transients from the switching stage of the supply can interfere with the operation of the lower-power more-sensitive control circuits. Therefore, internal screening and filtering are essential. However, external radiation is generally of more importance because, unlike the power supply control circuit which can be designed with these problems in mind, the external load and local equipment not connected to the supply may be affected by low levels of radiation and supply line noise. The situation is aggravated by the fact that suppression of transmitted noise may be made ineffective by radiated noise being picked up by the conductors and then retransmitted beyond the filtering components unless the positioning of these components with respect to screening is

carefully considered. The basic principles behind the suppression of r.f.i. in switched-mode power supplies, and the BSI and CISPR limits for radio frequency interference are discussed in Ref. 3. Screening details for the transformers used in the supply described here are given in the Appendices.

TURN-ON SEQUENCE

To prevent surge currents, and also to ensure that the control circuit is operative before the output voltage begins to rise, it is necessary to ensure the correct turn-on sequence. Fig. 15 shows the method of controlling the relevant auxiliary supply voltages. It is essential, both during turn-on and when the mains is removed, that the a.c. drive circuit does not operate unless the controller circuit is operating, and similarly that the switching transistors do not conduct unless both controller and drive circuits are operating. The turn-on control circuit in Fig. 15 ensures that the 15V line to the drive circuit is not connected unless the correct voltage is applied to the controller, and also that the inhibit input to the controller is held at zero unless the correct voltage is applied to the drive circuit.

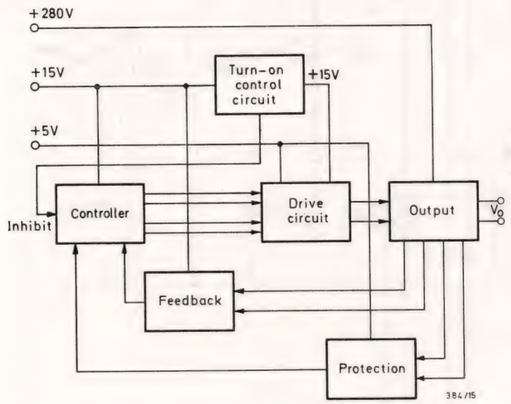


Fig. 15—Control of auxiliary voltages

The turn-on control circuit is shown in Fig. 16. At turn-on, the +5V and +15V drive lines gradually rise. Initially, the base of TR_1 rises with the 15V supply line whereas its emitter rises in proportion to a fraction of the voltage, determined by the ratio of R_2 and R_3. However, when the zener voltage of D_1 is reached, the base of TR_1 is clamped, while its emitter voltage continues to rise. When the emitter voltage reaches a value equal to the zener voltage of D_1 plus V_{BE}, TR_1 turns on and the current in R_4 and R_5 causes Schmitt trigger TR_2 and TR_3 to switch. By a suitable choice of values, any appropriate voltage can be chosen as the trip level.

This level-sensing circuit applies the drive voltage to the driver stage only when adequate voltage is available for correct operation of the controller. A similar circuit (right-hand side of Fig. 16) is used to sense that sufficient voltage is being applied to the driver before the inhibit to the controller is removed. In this way, no on-drive current can be applied to the output transistors unless all sections of the drive circuits are operating.

The integrator TR_{12}, TR_{13}, and C_2 provides a slow time-constant for the rise of the output voltage. To enable this circuit to reset rapidly, as is necessary to ensure correct ramp-up after a temporary power failure, the timing capacitor C_2 is rapidly discharged through D_3 and R_{24}.

COMPLETE 600W CIRCUIT

The complete circuit of the 600W switched-mode power supply is shown in Figs. 17a, 17b, and 17c. The numbers to the right of Fig. 17a, to the right and left of Fig. 17b, and to the left of Fig. 17c indicate how the parts of the circuit are connected. Compared with Fig. 1, the filters at the input and output are not included as these will depend on the particular application. Also, the overvoltage protection circuit of Fig. 14 is not shown as the positioning of this also depends on the application. Transformer and choke winding details are given in Appendices 2 to 5.

PERFORMANCE

The load regulation for an output voltage of 6·0V and a nominal a.c. input voltage of 240V is shown in Fig. 18. The measurements were made with remote sensing, the loads being connected to the circuit by 1·12m of cable.

The line regulation for an output voltage of 6·0V and the same remote sensing conditions is shown in Fig. 19. The measurements indicate that input voltage variations up to $\pm 15\%$ can be tolerated. However, much lower input voltages can be tolerated at reduced output power, particularly if an SMPS were used to provide the auxiliary voltages instead of the small 50Hz mains transformer used in this circuit.

The efficiency of the supply is shown in Fig. 20. It is almost independent of load current, the limit only being noticeable at less than 20% load where drive power requirements become a significant proportion of the output power. For practical load currents, the overall efficiency is greater than 60%.

The components of noise voltage at the output terminals are shown in Fig. 21. The corresponding values at a load connected to the supply by long cables will be substantially less because of the filtering effect of the cable inductance and the load capacitance. These measurements were taken with no high-frequency filters at the output terminals.

Packing density

The packing density of components in an SMPS can be specified in terms of size and weight. For the circuit described, the dimensional packing density is approximately 20ml/W (1·2in³/W). This figure compares favourably with that for conventional supplies, typically 100 to 200ml/W (6 to 12in³/W). The weight of the prototype is 14kg, which corresponds to 235g/W.

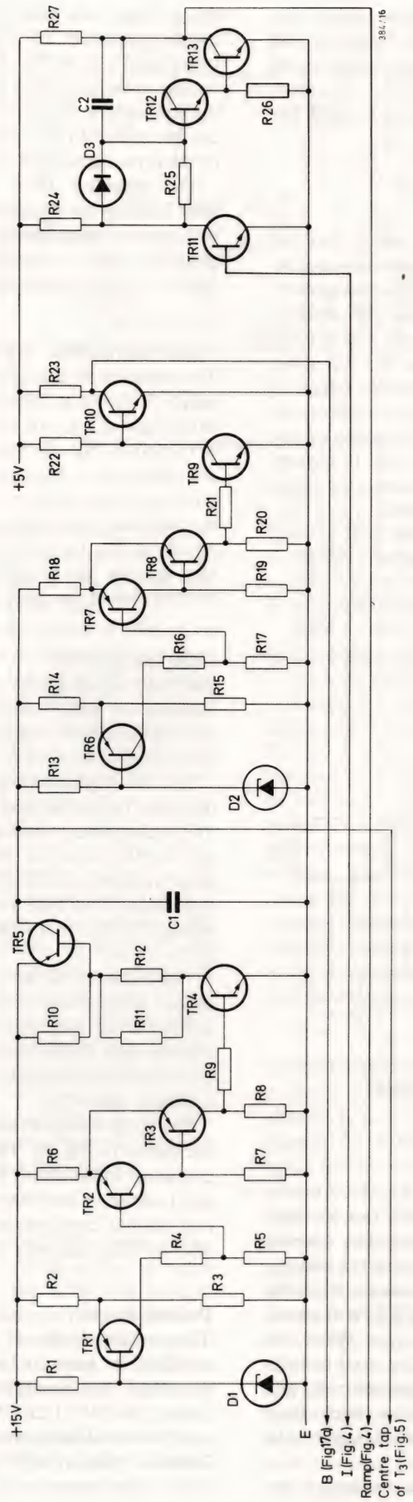


Fig. 16—Turn-on control circuit

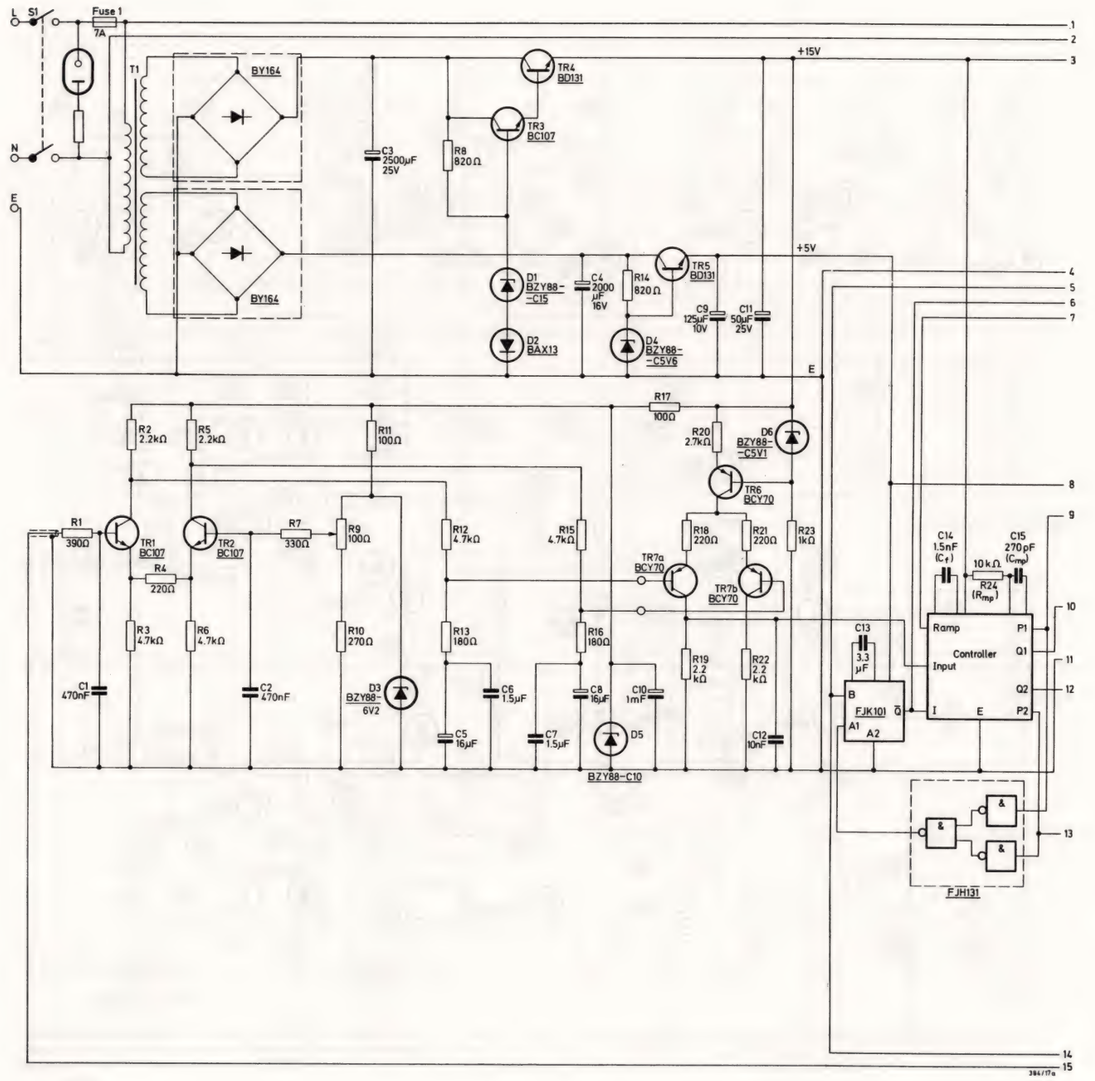


Fig. 17a—600W SMPS circuit (part a)

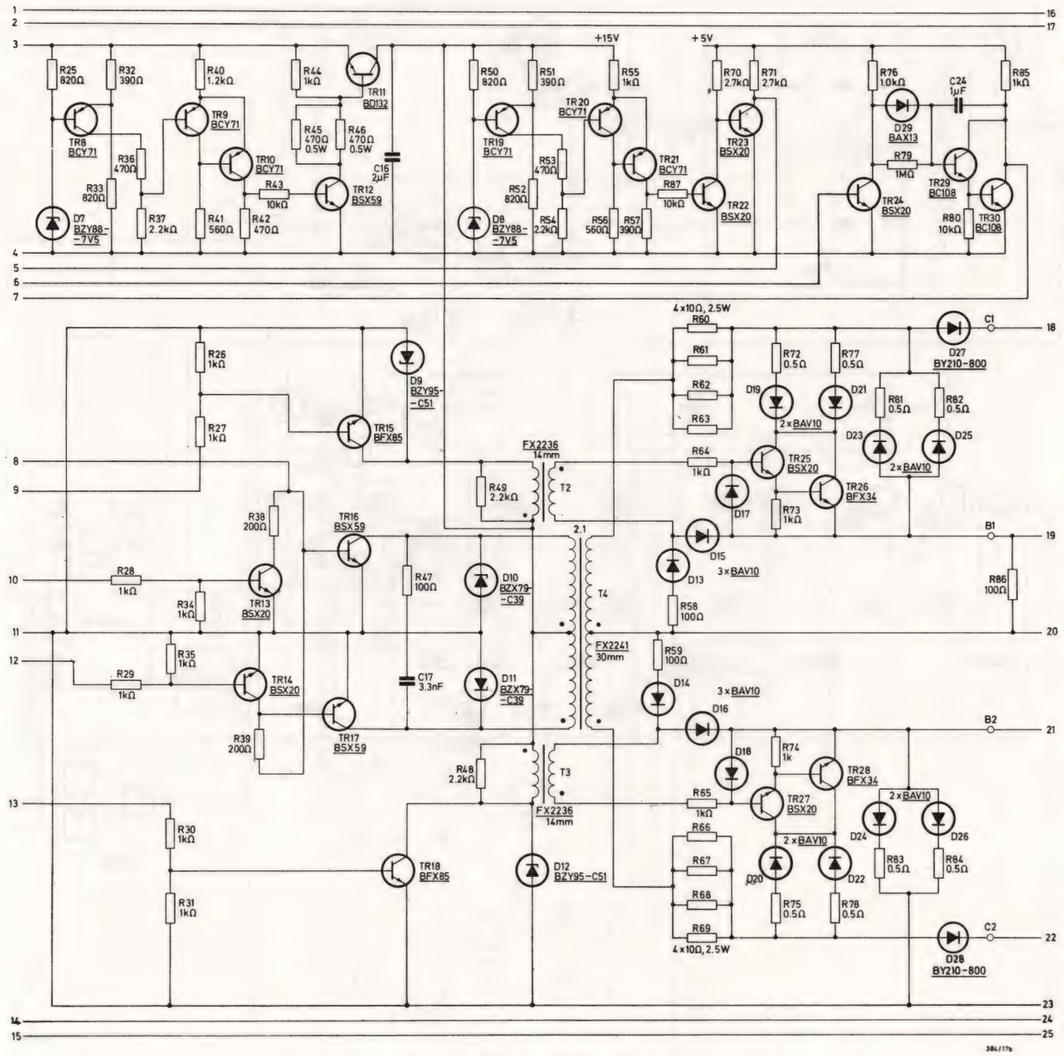


Fig. 17b—600W SMPS circuit (part b)

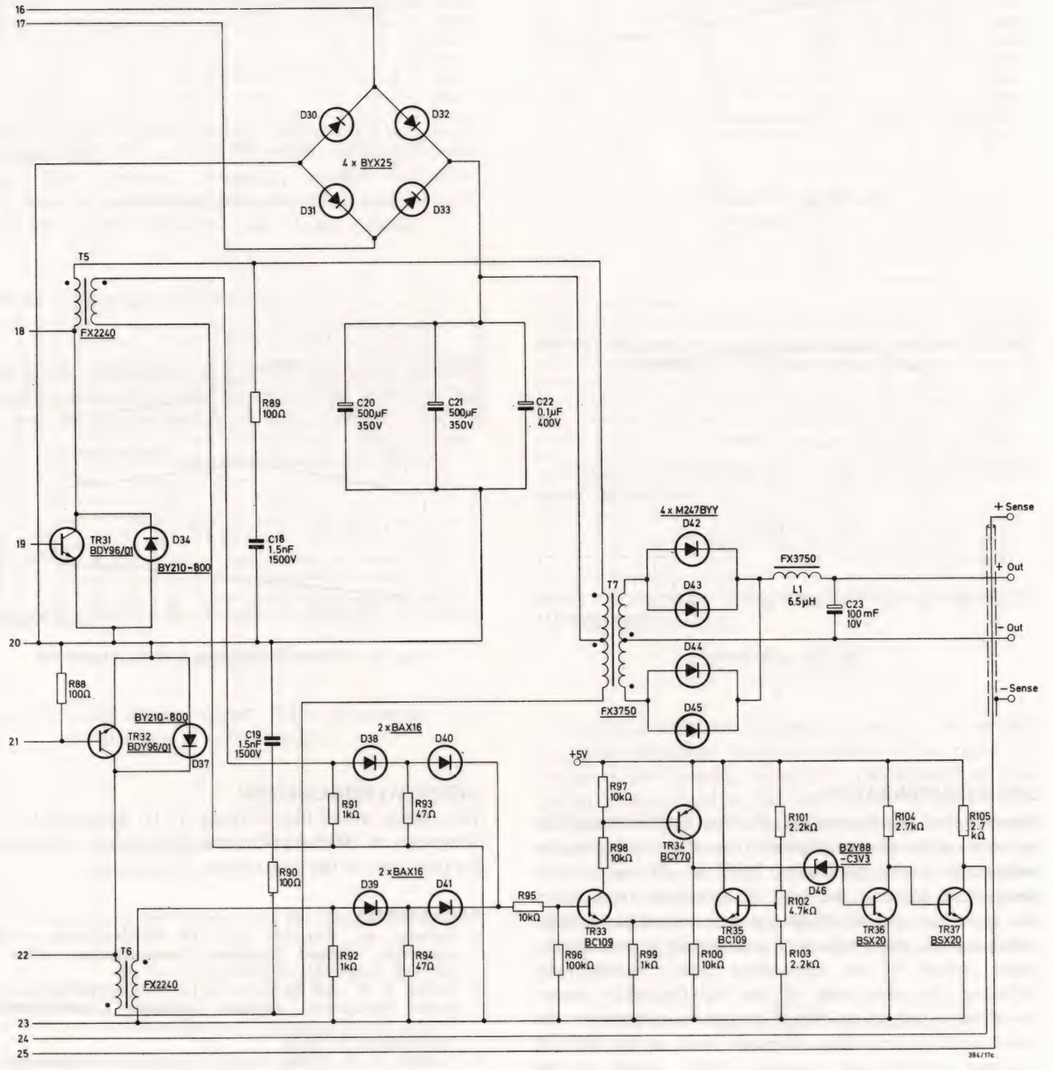


Fig. 17c—600W SMPS circuit (part c)

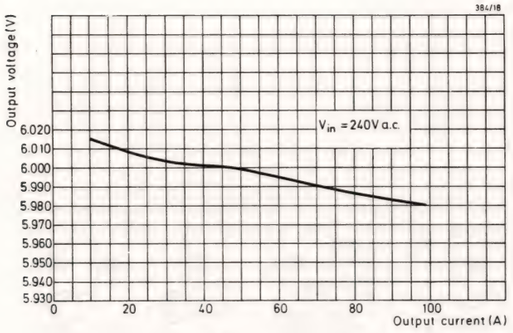


Fig. 18—Load regulation

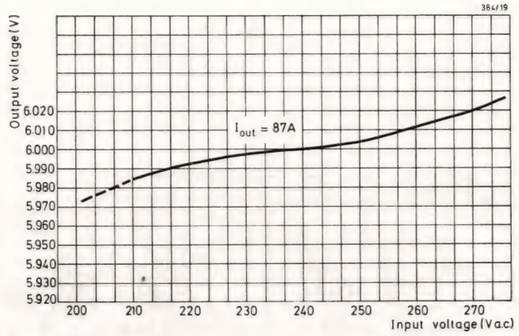


Fig. 19—Line regulation

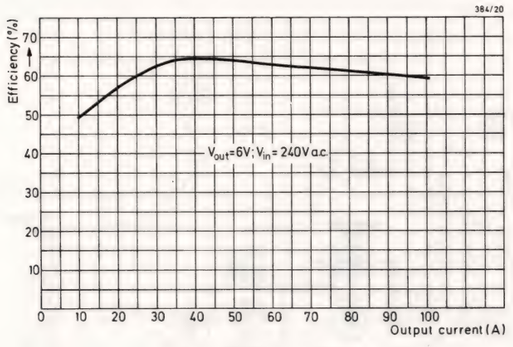


Fig. 20—Efficiency

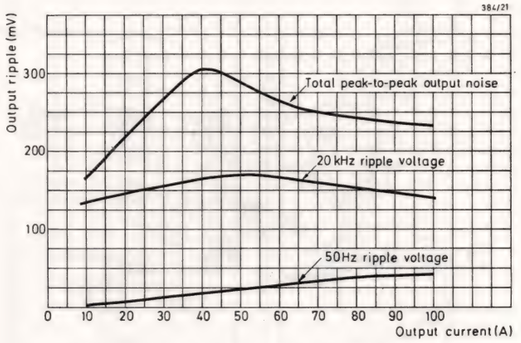


Fig. 21—Noise components at output terminals

50V D.C. OPERATION

The switched-mode power supply described in this article is intended for direct operation from the rectified mains voltage; that is, approximately 280V d.c. The same basic design can, however, be used for operation from lower d.c. input voltages. To obtain the same output power from a reduced d.c. input voltage, it is necessary to increase the input current by the appropriate factor. However, by reducing the turns ratio of the high-frequency output transformer and using output transistors suitable for the lower voltages and higher currents (such as the BDY90, V_{CE}max = 120V and I_{CM}max = 15A), much of the circuitry originally designed for mains drive can be utilised.

A prototype circuit operating from an unstabilised 50V d.c. input at a frequency of 50kHz has been constructed. The circuit produces 6V at 100A at an efficiency of about 70%, which compares favourably with the 20 to 30% obtainable with an equivalent series regulator circuit.

ACKNOWLEDGEMENTS

The author would like to thank T. H. Brown and J. R. Kinghorn of Mullard Central Application Laboratory for their help in the preparation of this article.

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5. BURGUM, F. J., 'Electrolytic capacitors for output filters of switched-mode power supplies: discussion of desirable characteristic', **Mullard Technical Communications,** Vol. 13, No. 123, July 1974, pages 125 to 140 (this issue). Reprinted as TP 1459.

APPENDIX 1
Output Transistor Dissipation

The dissipation in the output transistor results from three factors.

Firstly, the bottoming voltage during conduction gives rise to an average power loss P_1 of:

$$P_1 = I_c V_{CE(sat)} \times \frac{t_{on}}{\tau},$$

where I_c is the average collector current, and t_{on}/τ is the proportion of the period during which conduction takes place. The maximum dissipation therefore occurs at maximum pulse width, a typical pulse width being between 90 to 95% of the conduction time. Hence, typically,

$$P_1 = 0{\cdot}9\ I_c V_{CE(sat)},$$

or since the switching frequency $f_s = 1/\tau$,

$$P_1 \simeq I_c\ V_{CE(sat)}\ f_s t_{on}.$$

Secondly, some dissipation occurs during the transient switching edges. Simplified waveforms are shown in Fig. 22, and the transient dissipation P_2 is given by:

$$P_2 = P_{(\text{falling edge})} + P_{(\text{rising edge})},$$

$$= \frac{1}{\tau}\int_0^{t_f} VI\ dt + \frac{1}{\tau}\int_0^{t_r} VI\ dt.$$

But, for the falling edge, assuming a linear fall in current,

$$V = V_s\left(\frac{t_f - t}{t_f}\right)$$

where V_s is the supply voltage. This is because at $t = 0$, $V = V_s$, and at $t = t_f$, $V = 0$. Similarly,

$$I = I_c\frac{t}{t_f},$$

since at $t = 0$, $I = 0$, and at $t = t_f$, $I = I_c$.

Therefore, for the falling edge, the dissipation P_f is:

$$P_f = \frac{1}{\tau}\int_0^{t_f} V_s I_c\left(\frac{t_f - t}{t_f^2}\right)t\ dt,$$

$$= \frac{V_s I_c}{\tau}\left[\frac{t^2}{2t_f} - \frac{t^3}{3t_f^2}\right]_0^{t_f}$$

$$= \frac{V_s I_c\ t_f}{6\tau}.$$

Similarly, for the rising edge,

$$P_r = \frac{V_s I_c\ t_r}{6\tau}.$$

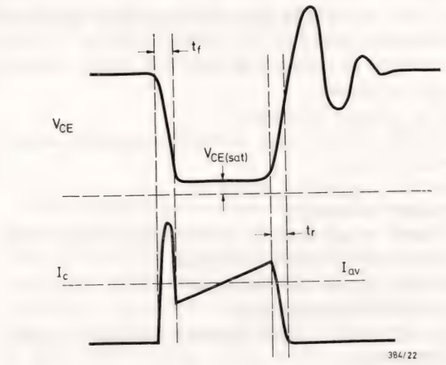

Fig. 22—Simplified waveforms of output transistor collector current and collector-emitter voltage

Therefore, the average power loss per cycle due to the switching transients is:

$$P_2 = \frac{V_s I_c(t_r + t_f)}{6\tau},$$

where τ is the period of one complete cycle. As the switching frequency $f_s = 1/\tau$,

$$P_2 = \frac{V_s I_c}{6}(t_r + t_f) f_s.$$

Finally, a transient dissipation occurs at the moment an output transistor turns on because of the rapid discharge of the damping capacitors. The amount of dissipation is dependent on the rate of fall of the collector voltage which is in turn dependent on the damping components. However, although the instantaneous power during this time may be quite high, the average power (averaged over one cycle) is normally negligible in comparison with the two forms of dissipation previously described. Therefore, the total average power dissipation in push-pull is:

$$P = 2 \times I_c f_s\left[V_s\frac{(t_f + t_r)}{6} + V_{CE(sat)} t_{on}\right].$$

Substituting worst-case figures, that is, $I_c = 5A$, $f_s = 25kHz$, $V_s = 374V$, $t_f = t_r = 100ns$, $V_{CE(sat)} = 2{\cdot}5V$, and $t_{on} = 20\mu s$, the total average power dissipation is:

$$P = 2 \times 5 \times 25 \times 10^3\left[\frac{(374 \times 200 \times 10^{-9})}{6} + 2{\cdot}5 \times 20 \times 10^{-6}\right],$$

$$= 15{\cdot}7W.$$

APPENDIX 2
Output Transformer (T_7, Fig. 17) Winding Details

The output transformer operates at 20 to 25kHz and utilises a pair of FX3750 cores which are designed specifically for SMPS operation. The primary winding is wound in two sections to minimise leakage inductance. Winding details are as follows:

1) Half of primary (winding 1)
   32+32 turns, 0·9mm diameter enamelled copper, bifilar-wound
2) Insulation, copper foil, insulation
3) Secondary (winding 2)
   4 turns, 32mm wide by 0·8mm thick copper strip, centre-tapped to give 2+2 turns
4) Insulation, copper foil, insulation
5) Half of primary (winding 3)
   32+32 turns, 0·9mm diameter enamelled copper, bifilar-wound

The copper foil is necessary for radiation suppression. No air gap is required.

APPENDIX 4
Current-sense Transformer (T_5 and T_6 in Fig. 17) Winding Details

Each current-sense transformer is wound on a 25mm pot core, type FX2240, using a former, type DT2179. Winding details are as follows:

1) 1 turn, 1·0mm diameter enamelled copper
2) Insulation, copper foil, insulation
3) 70 turns, 0·20mm diameter enamelled copper

APPENDIX 3
Output Filter Inductor (L_1, Fig. 17) Winding Details

The output filter inductor is wound on a pair of E-cores, type FX3750. Winding details are as follows:

9 turns, 32mm wide by 0·8mm thick, copper strip.

The total air gap between the cores should be 4·5mm; thus a 2·25mm gap is required between the core halves. This gives an inductance of about 6·5μH and allows a current of 130A (peak) to be carried without saturation.

The inductance can be slightly altered by changing the air gap. However, too great a reduction of the gap can give rise to core saturation at high d.c. components of current.

APPENDIX 5
Drive Transformer Winding Details

Push-pull transformer (T_4, Fig. 17)

Core: 30mm pot core, type FX2241
Former: DT2205

Windings are as follows:

1) 21+21 turns, 0·4mm enamelled copper, bifilar-wound
2) Insulation, copper foil, insulation
3) 21+21 turns, 0·56mm enamelled copper, bifilar-wound
4) Insulation, copper foil, insulation
5) 21+21 turns, 0·4mm enamelled copper, bifilar-wound

Pulse transformers (T_2 and T_3, Fig. 17)

Core: 14mm pot core, type FX2236
Former: DT2202

Windings are as follows:

1) 90 turns, 0·125mm enamelled copper
2) Insulation, copper foil, insulation
3) 45 turns, 0·18mm enamelled copper

Electrolytic capacitors for output filters of switched-mode power supplies: discussion of desirable characteristics

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UDC 621.316.825.4

An analysis of the technical requirements for the low-voltage electrolytic capacitors used in the smoothing circuits of flyback, forward, and push-pull converters of switched-mode power supplies is made. The conclusions are substantiated by reference to some practical measurements. From the results, the requirements for output capacitors for a representative selection of switched-mode power supplies are derived. The results indicate that the economic advantages of flyback power supplies are not maintained at low output voltages and high output currents, unless higher ripple voltages can be tolerated or a π-section filter used in place of a single capacitor. At low output voltages and high output currents, forward and push-pull converters must be used.

INTRODUCTION

Some of the technical requirements for output filter capacitors in switched-mode power supplies (SMPS) are sufficiently high values of (a) peak voltage rating and (b) ripple current rating, and sufficiently low values of (c) the equivalent series resistance (ESR) and (d) the equivalent series inductance (ESL) of the capacitor. Requirement (a) must obviously be chosen early in the design stage.

The output filter capacitor ESR and ESL have a much greater effect in a SMPS than in a conventional series regulator; the ESR because of the high peak capacitor currents found in some types of SMPS (notably the flyback converter), and the ESL because the frequency of ripple currents in a SMPS is usually of the order of 10^4 Hz, rather than 10^2 Hz as in a conventional power supply. Both of these parasitic elements have a deleterious effect on the level of output ripple from a SMPS, and also on the response to sudden changes in load.

Requirement (b), the capacitor ripple current rating, raises the question of whether the manufacturer's specification for the maximum ripple current in a given capacitor is for a peak or r.m.s. current; as will be shown, both may be calculated for the three main types of SMPS.

ANALYSIS OF OUTPUT FILTER CAPACITOR RIPPLE CURRENT AND VOLTAGE

The method used to determine the ripple current waveform in the output filter capacitor of a SMPS is that of analytic solution of the differential equations for a somewhat simplified equivalent circuit of the output stage of the supply. In the analysis of ripple currents, it is assumed that the supply has reached equilibrium through the feedback circuit.

The resistances (a.c. and d.c.) of transformer windings, and the effects of all stray capacitances, are ignored. It is expected that, in a well-designed SMPS, the winding resistances will be small compared with the reactances of the circuit inductances. It is also expected that the only effects of small stray capacitances in the circuit would be to slow down voltage edges, and to cause oscillations superimposed on the more slowly-varying waveforms. For either effect, the results of a calculation neglecting the influence of winding resistances and stray capacitances would give the worst possible values for peak ripple current and voltage. These approximations are validated by observations of several operational power supplies, in which the current waveforms are composed of segments which are all very nearly linear; the curvature due to resistances in the circuit is slight.

For similar reasons, core losses, and losses in active components, have been omitted from the analysis; any dissipation in the circuit tends to reduce the output ripple current.

In the following analysis, expressions for the ripple current waveforms in the output capacitor of each type of SMPS are derived, and the ripple voltages due to this ripple current passing through each of the three series elements of the output filter capacitor are calculated.

Forward converter

A representative circuit of the output stage of a forward converter is shown in Fig. 1. The output filter capacitor is assumed to have the equivalent circuit enclosed in the

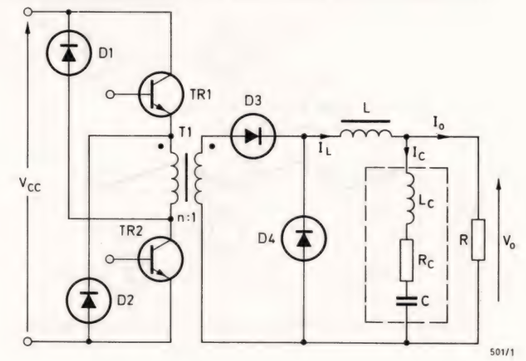


Fig. 1—Output stage of a forward converter

dotted box; L_C is the capacitor ESL, and R_C the ESR. It is assumed that the impedances of L_C, R_C, C, and the transformer secondary leakage inductance are small compared with the inductance of the smoothing choke L.

In the following calculations,

V_{CC} is the rectified and smoothed supply voltage (variable, for a nominal 240V a.c. mains supply from 210V to 400V d.c.; this range takes account of the maximum variation in r.m.s. mains voltage and of possible transient spikes and missing half-cycles of the mains);

V_o, I_o, are the required regulated output voltage and maximum output current;

n is the transformer primary-to-secondary turns-ratio;

$V'_{CC}=V_{CC}/n$ is the peak open-circuit transformer secondary voltage:

V_R is the forward voltage drop in one of the rectifier diodes D_3, D_4, plus the d.c. voltage drop across L at maximum I_o;

$V_s=V_o+V_R$.

Some of the voltage and current waveforms are shown in Fig. 2. Fig. 2a shows the current in the choke L as a function of time where;

t_a is the time during which transistors TR_1 and TR_2 are conducting;

t_b is the time during which they are turned off.

If f is the operating frequency, then

$$t_a+t_b = 1/f,$$

and the duty cycle is $\delta = ft_a$.

During time t_a, the voltage drop across the choke L is equal to $V'_{CC}-(V_o+V_R)=V'_{CC}-V_s$, and the current I_L in the choke is given by:

$$I_L = I_1+\frac{(V'_{CC}-V_s)}{L}t, \qquad (0\leqslant t\leqslant t_a)$$

where I_1 is the lowest value of I_L.

During the flywheel period t_b, D_4 is conducting, and the voltage across L must be equal to $(-V_o-V_R)=-V_s$ only.

Hence, during t_b,

$$I_L = I_2 -\frac{V_s}{L}\,(t-t_a), \qquad (t_a\leqslant t\leqslant 1/f)$$

where I_2 is the highest value reached by I_L.

The current in the choke must be a continuous function of time, and so:

$$I_2-I_1 = \frac{(V'_{CC}-V_s)}{L}t_a = \frac{V_s t_b}{L}.$$

Therefore, as expected, to maintain an output voltage V_o,

$$\delta = ft_a = V_s/V'_{CC}.$$

Substituting for t_a in the equation for (I_2-I_1),

$$I_2-I_1 = \frac{(V'_{CC}-V_s)}{fLV'_{CC}}V_s = \Delta I_L,$$

which is the peak-to-peak change in I_L.

The current I_C in the output capacitor has no d.c. component and so, if the load is constant, the capacitor current must vary between $\pm\Delta I_L/2$.

The peak capacitor current is therefore:

$$I_{C(pk)} = \frac{(V'_{CC}-V_s)}{2\,f\,LV'_{CC}}V_s.$$

The r.m.s. capacitor current is also given by:

$$I_{r.m.s.} = I_{C(pk)}/\sqrt{3}.$$

If this current, $I_C = I_L-I_o$, varying between $\pm\Delta I_L/2$

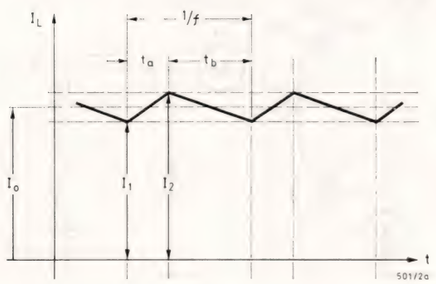


Fig. 2a—Forward converter inductor current

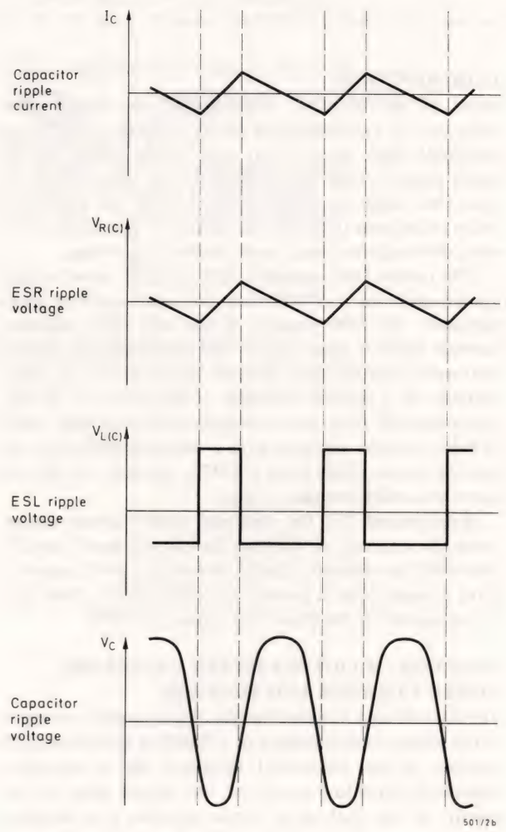


Fig. 2b—Capacitor ripple current and ripple voltages

passes through the three equivalent series elements of the output filter capacitor, then the ripple voltage on each of the three components consists of:

Resistive part: voltage waveform is given by:

$$V_{R(C)} = I_C R_C,$$

and the peak-to-peak value of this is:

$$\Delta V_{R(C)} = \frac{(V'_{CC}-V_s)V_s R_C}{fLV'_{CC}}.$$

Inductive part: voltage waveform is given by:

$$V_{L(C)} = L_C\frac{dI_C}{dt},$$

and the peak-to-peak value of this is:

$$\Delta V_{L(C)} = V'_{CC}\frac{L_C}{L}.$$

Capacitive part: voltage waveform is given by:

$$V_C = \frac{1}{C}\int_{t_1}^{t} I_C\,dt,$$

where V_C at t_1 is zero, and the peak-to-peak value of this is:

$$\Delta V_C = \frac{1}{C}\frac{(V'_{CC}-V_s)V_s}{8f^2LV'_{CC}}.$$

The inductive and resistive components may be directly added because, as shown in Fig. 2b, the peak values of both waveforms coincide temporarily.

Push-pull circuit

A simplified representative push-pull output circuit is shown in Fig. 3. The analysis of this circuit is similar to that of the simplified forward converter of the previous Section with the exception that the effective duty cycle can approach 100%, and the ripple current frequency in the choke is twice the driving frequency f.

In the push-pull circuit:

$$\Delta V_{R(C)} = \frac{R_C(V'_{CC}-V_s)V_s}{2fLV'_{CC}},$$

$$\Delta V_{L(C)} = \frac{L_C V'_{CC}}{L},$$

$$\Delta V_C = \frac{1}{C}\frac{(V'_{CC}-V_s)V_s}{32Lf^2V'_{CC}},$$

$$I_{C(pk)} = \frac{(V'_{CC}-V_s)V_s}{4fLV'_{CC}},$$

and

$$I_{r.m.s.} = I_{C(pk)}/\sqrt{3}, \text{ as before.}$$

Flyback converter

The standard output circuit is considered, and the effect of adding a single-stage LC low-pass filter to the output is discussed.

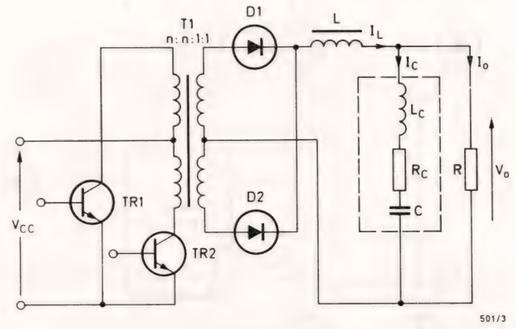


Fig. 3—Push-pull converter output circuit

Flyback converter with standard output circuit

A circuit for a typical flyback converter output stage is shown in Fig. 4. This type of SMPS functions in a different manner from the two circuits previously discussed. Energy is stored in the transformer while the transistors TR_1 and TR_2 are conducting, and is only transferred to the output capacitor when the transistors turn off. Also, no smoothing choke of appreciable magnitude can be used between the output diode and the filter capacitor, so the effects of the leakage inductance of the transformer become the dominant factors in determining the rates of change of current in the capacitor.

Fig. 5 shows the circuit of Fig. 4 re-drawn. The transformer is represented by primary and secondary leakage inductances and a shunt magnetisation inductance, with voltage and current transformation effected by an ideal transformer (with infinite impedances). The turns-ratio is the same as that of the original transformer.

L_p and L_s are the inductances of the primary and secondary windings of the original transformer; k is the coupling constant, so that the mutual inductance is given by:

$$M = k\sqrt{(L_p L_s)}, \qquad k \leqslant 1.$$

If the turns-ratio of the transformer is n : 1, the

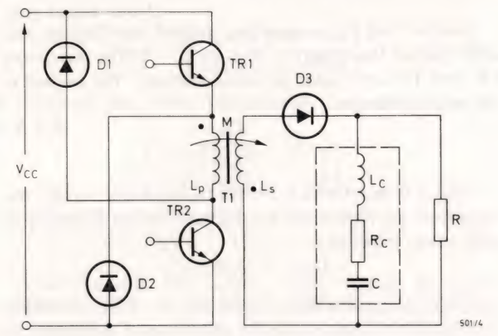


Fig. 4—Flyback converter output stage

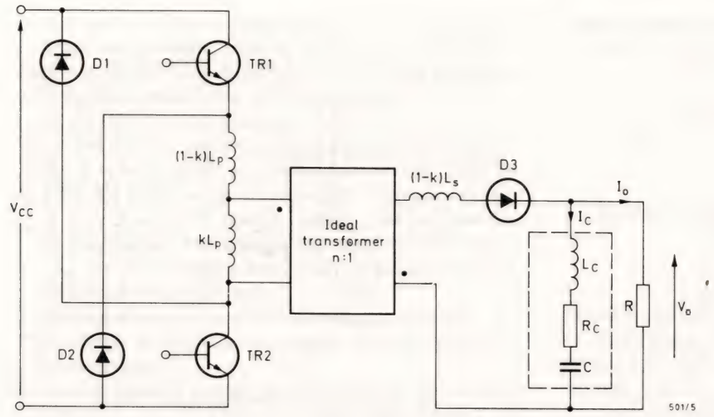


Fig. 5—Flyback converter with imperfect transformer coupling

primary and secondary inductances are related by:

$$L_p = n^2 L_s.$$

The real transformer is thus represented by an ideal transformer of ratio n, with a magnetisation inductance kL_p across its primary (or kL_s across its secondary), and with leakage inductances of $(1-k)L_p$ and $(1-k)L_s$ in series with the primary and secondary.

Let:

V'_{CC} = V_{CC}/n = peak open-circuit secondary voltage
V_o = output voltage
I_o = output current
V_R = forward voltage drop of diode D_3
V_s = V_o+V_R
I_p = primary current
I_s = secondary current
I'_p = primary current reflected in the secondary; that is, $I'_p = nI_p$
$I_{p(pk)}$ = peak value of I_p
$I_{s(pk)}$ = peak value of I_s
$I'_{p(pk)}$ = peak value of I'_p

Assume that the system has reached equilibrium, and at the start of the cycle ($t = 0$) $I_p = I_s = 0$. The transistors TR_1 and TR_2 are turned on simultaneously. The current in the primary rises as:

$$I_p = \frac{V_{CC}t}{L_p}.$$

After a time interval t_a (where ft_a is the duty cycle), the transistors are turned off; the primary current is then at its peak value, given by:

$$I_{p(pk)} = V_{CC}t_a/L_p\,. \qquad \ldots(1)$$

When the transistors turn off, I_p must decrease, causing the voltage across the primary and secondary to reverse until the diodes D_1 and D_2 can conduct. The equivalent circuit of the secondary at this moment in time is shown in Fig. 6, with initial currents $I'_p = I'_{p(pk)}$, $I_s = 0$.

Analysis shows that the reflected primary current I'_p decreases as:

$$I'_p = I'_{p(pk)} - \left[\frac{(V'_{CC}-kV_s)}{(1-k^2)L_s}\right](t-t_a)\,, \qquad \ldots(2)$$

while the secondary current I_s increases as:

$$I_s = \left[\frac{(kV'_{CC}-V_s)}{(1-k^2)L_s}\right](t-t_a) \quad (t_a \leqslant t \leqslant t_a+t_b) \qquad \ldots(3)$$

It is noted that from Eq. 1,

$$I'_{p(pk)} = V'_{CC}t_a/L_s\,. \qquad \ldots(1a)$$

The primary current reaches zero after a time interval t_b; the diodes D_1 and D_2 cease to conduct. Time t_b is therefore given by:

$$t_b = \frac{I'_{p(pk)}(1-k^2)L_s}{(V'_{CC}-kV_s)},$$

and combining this with Eq. 1a,

$$t_b = \frac{t_a V'_{CC}(1-k^2)}{(V'_{CC}-kV_s)}. \qquad \ldots(4)$$

At the end of this period t_b, the secondary current I_s has reached its maximum value given by:

$$I_{s(pk)} = I'_{p(pk)}\frac{(kV'_{CC}-V_s)}{(V'_{CC}-kV_s)}. \qquad \ldots(5)$$

While the transistors TR_1 and TR_2 are turned off, and the diodes D_1 and D_2 are not conducting, no current can flow in the primary; the primary winding can thus be

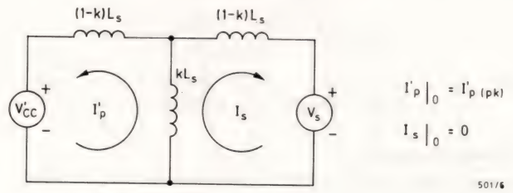


Fig. 6—Equivalent circuit during t_b

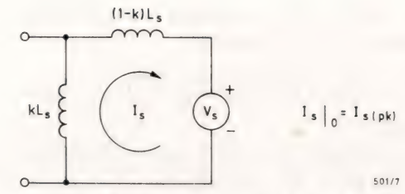


Fig. 7—Equivalent circuit during t_c

ignored, and the equivalent circuit of the secondary can be re-drawn as shown in Fig. 7, with an initial current $I_s = I_{s(pk)}$. The secondary current thus decreases as:

$$I_s = I_{s(pk)} - \frac{V_s}{L_s}(t-t_a-t_b).$$

I_s reaches zero after a time interval t_c, where:

$$t_c = I_{s(pk)}L_s/V_s.$$

By Eq. 5, this gives:

$$t_c = I'_{p(pk)}\frac{(kV'_{CC}-V_s)L_s}{(V'_{CC}-kV_s)V_s},$$

and, by Eq. 1a:

$$t_c = \frac{V'_{CC}}{V_s}\,\frac{(kV'_{CC}-V_s)}{(V'_{CC}-kV_s)}\,t_a. \qquad \ldots(6)$$

A further period t_d follows before the transistors TR_1 and TR_2 are turned on again, and hence:

$$t_a+t_b+t_c+t_d = 1/f,$$

where f is the operating frequency.

The resulting current waveforms in the primary and secondary windings are shown in Fig. 8.

The mean value of the secondary current must be equal to the mean value of the supply output current I_o (that is, the capacitor carries no d.c. current). The capacitor current waveform may thus be drawn as shown in the top graph of Fig. 9; this waveform is the same as that in the transformer secondary, but less a constant amount I_o. The mean value of the waveform over an integral number of periods is zero.

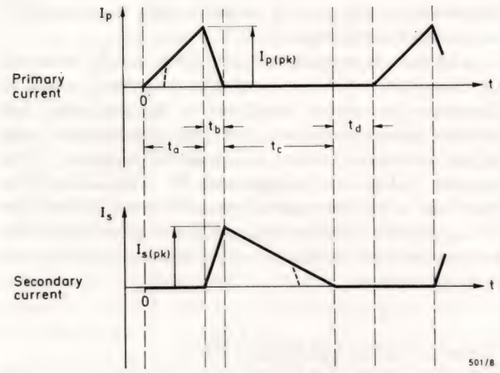


Fig. 8—Primary and secondary currents in the flyback transformer

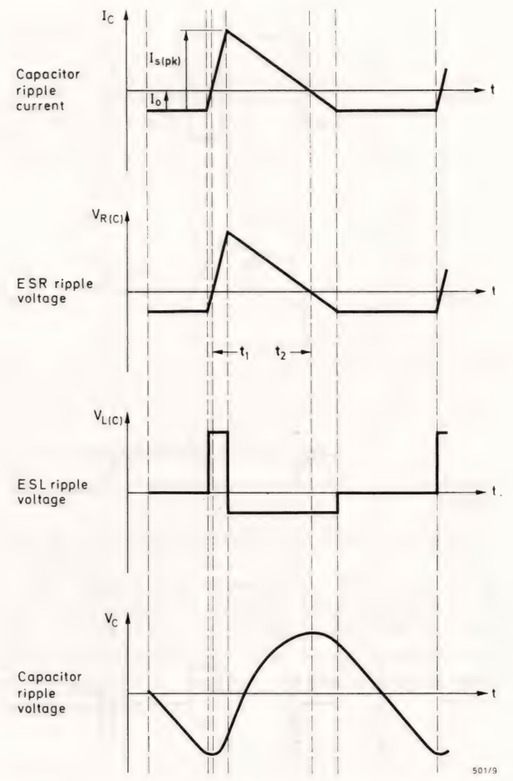


Fig. 9—Waveforms of ripple current and ripple voltage

The mean value of the secondary current I_s is:

$$I_o = \frac{f}{2}I_{s(pk)}(t_b+t_c),$$

and, using Eqs. 1, 4, and 6, the value of t_a needed to sustain this output current is:

$$t_a = \left[\frac{2I_oL_sV_s(V'_{CC}-kV_s)}{kfV'^2_{CC}(kV'_{CC}-V_s)}\right]^{\frac{1}{2}}. \qquad \ldots(7)$$

Using Eqs. 5 and 1,

$$I_{s(pk)} = \left[\frac{2I_oV_s(kV'_{CC}-V_s)}{kfL_s(V'_{CC}-kV_s)}\right]^{\frac{1}{2}}. \qquad \ldots(8)$$

It is noted that these relationships only hold true if $t_d \leqslant 0$ or,

$$f\left[\frac{2I_oL_sV_s(V'_{CC}-kV_s)}{fkV'^2_{CC}(kV'_{CC}-V_s)}\right]^{\frac{1}{2}} \times$$

$$\times\left[1+\frac{V'_{CC}(1-k^2)}{(V'_{CC}-kV_s)}+\frac{V'_{CC}(kV'_{CC}-V_s)}{V_s(V'_{CC}-kV_s)}\right] \leqslant 1. \qquad \ldots(9)$$

Assuming that the output ripple voltage is small compared with V_o, and therefore that the output current I_o is essentially constant, the capacitor current I_C becomes

$$I_C = I_s - I_o,$$

as shown in Fig. 9.

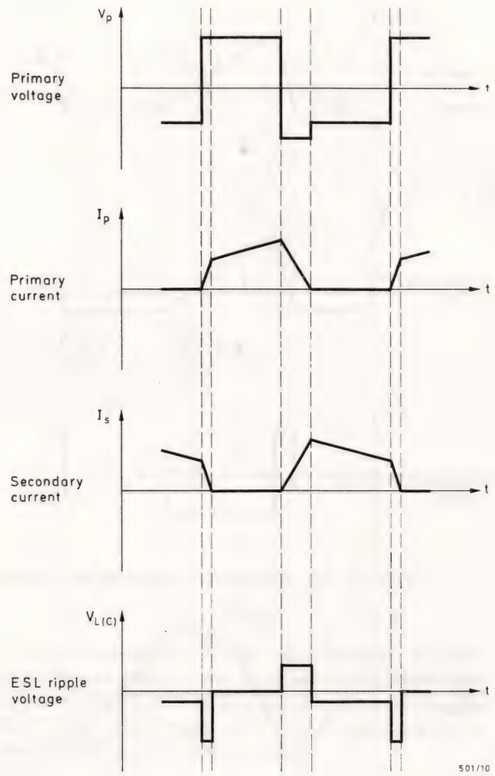


Fig. 10—ESL ripple when flyback converter periods overlap

Consequently, the ripple voltage waveforms of the ESR, ESL, and pure capacitive elements of the output filter capacitor approximate those shown in the three lower graphs of Fig 9. The three ripple voltage waveforms are:

Resistive Part: $V_{R(C)}=I_C R_C$

Peak-to-peak value of $V_{R(C)}$ is:

$$\Delta V_{R(C)}=R_C\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}},$$

where the parameters $X=(kV'_{CC}-V_s)$ and $Y=(V'_{CC}-kV_s)$ are introduced for convenience.

Inductive part: $V_{L(C)}=L_C\dfrac{dI_C}{dt}$

Peak-to-peak value of $V_{L(C)}$ is:

$$\Delta V_{L(C)}=\frac{L_C}{L_s}\left[\frac{X}{(1-k^2)}+V_s\right].$$

Capacitive part:

$$\Delta V_C=\frac{1}{C}\int_{t_1}^{t_2} I_C\,dt,$$

where t_1 and t_2 are two successive points at which $I_C=0$, as shown in Fig. 9. Therefore,

$$\Delta V_C=\tfrac{1}{2}(t_b+t_c)\frac{(I_{s(pk)}-I_o)}{I_s}(I_{s(pk)}-I_o),$$

which gives

$$\Delta V_C=\frac{kI_oL_s}{2C}\left[\frac{1-k^2}{X}+\frac{1}{V_s}\right]\left[\frac{2V_sX}{fL_sYk}-2\left(\frac{2V_sI_oX}{kfL_sY}\right)^{\frac{1}{2}}+I_o\right].$$

The peak capacitor current is equal to $I_{s(pk)}-I_o$. Hence,

$$I_{C(pk)}=\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}-I_o.$$

When the relationship of Eq. 9 is not satisfied, that is when the transistors TR_1 and TR_2 turn on before the transformer secondary current has decayed to zero, the ripple voltage may show a large increase. This increase is due almost entirely to the ESL of the output filter capacitor, and arises in the following way.

When the transistors TR_1 and TR_2 are turned on, the secondary current falls rapidly as the secondary voltage reverses, and the primary current rises rapidly (Fig. 10). The slope of the decreasing secondary current I_s is very much greater (more negative) than at any other point in the cycle, and this results in a negative-going voltage pulse across the ESL of the output capacitor.

The secondary current during the period in which the primary current is increasing rapidly is given by:

$$I_s=I_2-\frac{(kV'_{CC}+V_s)}{(1-k^2)L_s}\,t,$$

where $I_s=I_2$ and $t=0$ at the instant of turn-on of the two transistors. Therefore,

$$V_{L(C)}=L_C\frac{dI_C}{dt}=-\frac{(kV'_{CC}+V_s)L_C}{(1-k^2)L_s}.$$

The peak-to-peak ESL ripple voltage thus becomes:

$$\Delta V_{L(C)}=\frac{2L_CkV'_{CC}}{L_s\,(1-k^2)},$$

which is equal to twice the on-load secondary voltage, attenuated by the ratio of capacitor ESL to transformer secondary leakage inductance.

Although the magnitude of $\Delta V_{L(C)}$ has greatly increased, the magnitude of $\Delta V_{R(C)}$ and ΔV_C may be expected to decrease; the current waveform in the secondary has become more rectangular, and the peak-to-mean ratio of the secondary current is substantially reduced. This suggests that the above expression for $\Delta V_{L(C)}$ should be combined with the expressions previously derived for $\Delta V_{R(C)}$ and ΔV_C in circuits in which it is expected that the primary will be turned on while the secondary is still carrying current.

Flyback converter with output π-filter

The output stage of a flyback converter may be modified by the addition of an LC low-pass filter, to attenuate the ripple voltage, and to thus permit capacitors with higher values of ESL and ESR to be used (Fig. 11).

A rigorous analysis of this output circuit is extremely

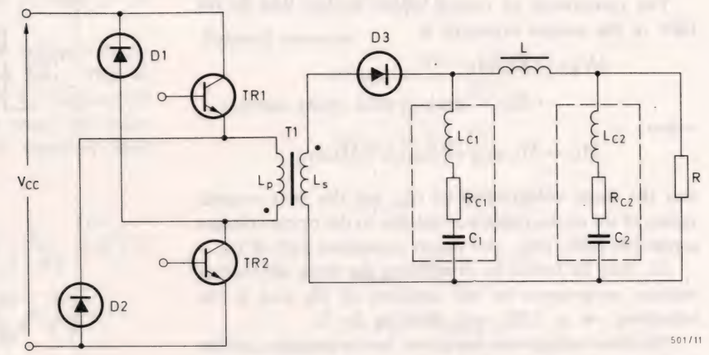


Fig. 11—Flyback converter with LC filter

difficult; however, certain approximations may be made, as now explained.

The first approximation is that the voltage at the cathode of D_3 (Fig. 11) is exactly the same as it would be in the circuits (Figs. 4 and 5) without the LC filter. This approximation is valid in relation to the mathematics of the preceding section, in as much as the analysis treated the resistive load as a constant current sink (which is true if the ripple voltage is small and the load constant). In Fig. 11, the effect of the smoothing choke L is to reduce still further the variations in current, or to allow the same current changes as before but with a larger ripple voltage on the first of the two capacitors. If the analysis is valid for the simple flyback circuit, it is therefore equally valid for the flyback converter with an added LC filter.

A corollary of this approximation is that the output LC filter and load may be treated as an independent LCR network, fed by a zero-impedance voltage source with an a.c. waveform the same as that derived for the output ripple voltage of the basic flyback circuit.

The second approximation is that the values derived for the peak-to-peak ripple voltage across the output capacitor of the simple flyback circuit may also be used in Fig 11 for the voltage at the junction of D_3 and L. The ripple voltage at this junction may not necessarily be small compared with the d.c. voltage on the capacitor C_1. This is a reasonable assumption, since the effects of larger voltage variations on the capacitor will simply decrease the rates of change of current in the transformer secondary and therefore decrease the ripple voltage. The equations derived in the preceding section will thus always give larger values of ripple voltage at this junction than will occur in practice, the theory becoming more accurate at small values of L_{C1} and R_{C1}.

The third approximation is that the voltage variations across the output capacitor C_2 (Fig. 11) are small compared with the voltage variations on the capacitor C_1, so that the alternating component of voltage dropped across L is approximately the same as the alternating voltage appearing at the positive connection of the first capacitor. This is reasonable, because of the smoothing effect of the choke L.

The ripple voltage appearing on the output, at the junction of L and C_2, will have components due to the ESL and ESR of C_2, together with a component due to the purely capacitive part of C_2. If i_L is the alternating part of the current in L, and v_o is the alternating part of the output voltage, then:

$$v_o=i_LR_{C2}+L_{C2}\frac{di_L}{dt}+\frac{1}{C_2}\int_0^t i_L\,dt, \qquad \ldots(10)$$

$$=v_{R2}+v_{L2}+v_{C2}.$$

These three components of ripple voltage can be calculated separately. The second component v_{L2} is the easiest to derive because the value of di_L/dt is equal to the voltage difference across L divided by the value of L. Thus the peak-to-peak value of this component of the output ripple voltage will be:

$$\Delta V_{L2}=\frac{L_{C2}}{L}\Delta V_1,$$

where ΔV_1 is the peak-to-peak voltage excursion on the cathode of D_3. Hence, using the results on p. 130,

$$\Delta V_{L2}=\frac{L_{C2}}{L}\left\{R_{C1}\left[\frac{2I_oV_sX}{kf\,L_sY}\right]^{\frac{1}{2}}+\right.$$

$$+\frac{L_{C1}}{L_s}\left[\frac{X}{(1-k^2)}+V_s\right]+$$

$$\left.+\frac{I_oL_s}{2C_1}\left[\frac{(1-k^2)}{X}+\frac{1}{V_s}\right]\left(\frac{2V_sX}{fL_sYk}-2\left[\frac{2V_sI_oX}{kfL_sY}\right]^{\frac{1}{2}}+I_o\right)\right\}$$

$\ldots(11)$

where $X=(kV'_{CC}-V_s)$ and $Y=(V'_{CC}-kV_s)$, and all symbols have the same meaning as in the preceding section, except that L_{C1}, R_{C1}, C_1 represent the components of the first capacitor, whereas L_{C2}, R_{C2}, and C_2 represent the components of the second capacitor.

The component of output ripple voltage due to the ESR of the output capacitor is

$$\Delta V_{R2} = R_{C2}\Delta I_L$$
$$= R_{C2} \times \text{(peak-to-peak choke current)},$$

where:

$$\Delta I_L = \Delta I_{L(RC1)} + \Delta I_{L(LC1)} + \Delta I_{L(C1)},$$

and the three components of ΔI_L are the peak-to-peak values of the choke ripple current due to the ripple voltages across the ESR, ESL, and purely capacitive part of C_1.

ΔI_L may be found by integrating the three alternating voltage components at the junction of D_3 and L (as calculated on p. 130), and dividing by L.

The three voltages are integrated here separately, and the peak-to-peak values of current are added, without reference to their relative phase; this gives, in all circumstances, an absolute maximum value for ripple voltage.

The voltage component across L_{C1} is a squarewave (Fig. 9). Expressions were derived in the preceding section to give the amplitudes and durations of the sections of this waveform. A simple integration gives that part of the peak-to-peak choke current due to L_{C1} as:

$$\Delta I_{L(LC1)} = \frac{L_{C1}}{L}\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}. \qquad \ldots(12)$$

The component of ripple voltage appearing across R_{C1} is a triangular wave, as shown in Fig. 9. This is integrated, and the peak-to-peak change in I_L due to R_{C1} becomes:

$$\Delta I_{L(RC1)} = \frac{R_CI_s}{2L}\left(\frac{1-k^2}{X}+\frac{1}{V_s}\right)\times$$
$$\times\left(\frac{2I_oV_sX}{kfL_sY}-2I_o\left[\frac{2I_oV_sX}{fL_sYk}\right]^{\frac{1}{2}}+I_o^2\right). \qquad \ldots(13)$$

The component of ripple voltage on the first capacitor (C_1) due to its purely capacitive part is as shown in Fig. 9, and contains two quadratic sections and a linear part. Another assumption made here to simplify the working is that the rising edge of the secondary current waveform is vertical (as though there were no leakage inductance). The current waveform for C_1 may be treated as the sawtooth wave shown in Fig. 12. A further simplification can be made when the durations of the various portions of this waveform are considered. It should first be noted that the power supply must be able to operate even when the rectified smoothed mains is at its lowest possible value. When the mains is at minimum,

$$kV'_{CC} \geqslant V_s;$$

that is, the diode D_3 is still forward-biased. Accordingly, the period t_a (the on-time of the transformer primary) is approximately equal to the off-time (the theoretical limit of 50% duty cycle). To ensure maximum output current for a given peak diode current, the secondary inductance must be such that the secondary current reaches zero just before the transistors are turned on again. Consequently, at minimum mains voltage, t_a must $\simeq t_c$ and $t_c \simeq 1/2f$.

When the mains is at a higher value than the minimum, t_a decreases, but the peak secondary current, and t_c, remain constant if the load is constant. Hence, $t_c \leqslant 1/2f$,

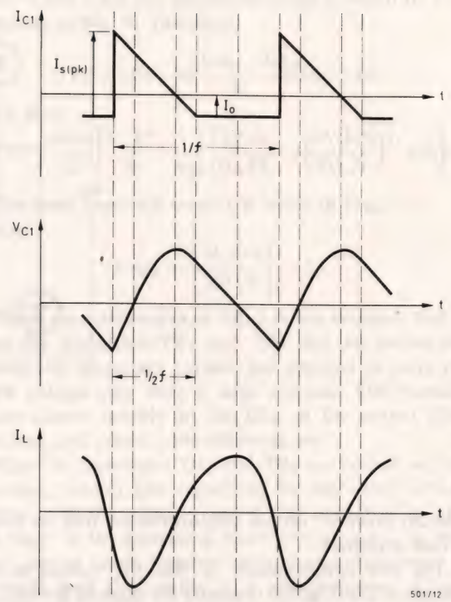


Fig. 12—Approximate waveforms of ripple current and ripple voltage

and the maximum ripple occurs at maximum output current, when $t_c = 1/2f$.

With the triangular wave shown in Fig. 12, the mean output current of the circuit must be equal to the mean secondary current, and therefore the peak secondary current is given by:

$$I_{s(pk)} = 4I_o.$$

This waveform may be defined by the equation:

$$I_{C1} = 3I_o - 8I_oft \quad (0 \leqslant ft \leqslant \tfrac{1}{2})$$
$$I_{C1} = -I_o \qquad (\tfrac{1}{2} \leqslant ft \leqslant 1).$$

This can be integrated once to give the voltage on the purely capacitive part of C_1, and again to give the current waveform in L due to this voltage.

Hence,

$$\Delta I_{L(C1)} = \frac{0{\cdot}0764\ R_{C1}I_o}{f^2\,C_1\,L}. \qquad \ldots(14)$$

Eqs. 12, 13, and 14 when added together give an absolute maximum current change in L, and the result multiplied by R_{C2} gives the maximum ripple voltage of the ESR of the output capacitor C_2; hence:

$$\Delta V_{R(C2)} = R_{C2}\left\{\frac{L_{C1}}{L}\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+\right.$$
$$+\frac{R_{C1}L_s}{2L}\left(\frac{1-k^2}{X}+\frac{1}{V_s}\right)\times$$
$$\times\left(\frac{2I_oV_sX}{kfL_sY}2I_o\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+I_o^2\right)+$$
$$\left.+\frac{0{\cdot}0764\ R_{C1}I_o}{f^2C_1L}\right\}. \qquad \ldots(15)$$

The result of adding Eqs. 11 and 15 is the maximum ripple voltage on the output capacitor C_2 due to its combined ESL and ESR.

The third term in Eq. 10, the ripple voltage due to the capacitive part of C_2, is neglected here. This is because, as will be shown, the value of C_2 required to achieve low ripple is considerably less than the value required to achieve good response to transient load changes.

Adding Eqs. 11 and 15:

$$\Delta V_o = \frac{1}{L}\left\{R_{C1}L_{C2}\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+\frac{L_{C2}L_{C1}}{L_s}\left(\frac{X}{(1-k^2)}+V_s\right)+\right.$$
$$+R_{C2}L_{C1}\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+\frac{R_{C2}L_s}{2}\left(\frac{1-k^2}{X}+\frac{1}{V}\right)\times$$
$$\times\left(\frac{2I_oV_sX}{kfL_sY}-2I_o\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+I_o^2\right)\Bigg\}+$$
$$+\frac{1}{L_{C1}}\left\{\frac{I_oL_sL_{C2}}{2}\left(\frac{1-k^2}{X}+\frac{1}{V_s}\right)\times\right.$$
$$\times\left(\frac{2V_sX}{fL_sYk}-2\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+I_o\right)+$$
$$\left.+0{\cdot}0764\ \frac{R_{C1}R_{C2}I_o}{f^2}\right\}. \qquad \ldots(16)$$

In practice, C_1 and C_2 may be of the same type and have comparable values of ESL and ESR; in this instance the above equation may be somewhat simplified. When the values of L_C and R_C are defined, only L and C_1 need be calculated from Eq. 16, and C_2 may be found by considering transient load changes. This equation has been divided into two parts, one reflecting the effects of the ESL and ESR of both capacitors, and one reflecting the effect of the pure capacitive part of C_1. It is suggested that this rather arbitrary division is used to separate the calculations of L and C_1. First, the part of Eq. 16 not containing C_1 may be equated to two-thirds of the required maximum ripple voltage, and a value for L obtained. Second, the part of Eq. 16 which does contain C_1 may be equated to one-third of the required maximum ripple voltage, and a value found for C_1 using the value of L just calculated; that is:

$$\frac{2}{3}\Delta V_o = \frac{1}{L}\left\{2R_CL_C\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+\frac{L_C^2}{L_s}\left[\frac{X}{1-k^2}+V_s\right]+\right.$$
$$+\frac{R_CL_s}{2}\left[\frac{1-k^2}{X}+\frac{1}{V_s}\right]\times$$
$$\left.\times\left(\frac{2I_oV_sX}{kfL_sY}-2I_o\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+I_o^2\right)\right\}, \qquad \ldots(17a)$$

and

$$\frac{1}{3}\Delta V_o = \frac{1}{L_{C1}}\left\{\frac{I_oL_sL_C}{2}\left(\frac{1-k^2}{X}+\frac{1}{V_s}\right)\times\right.$$
$$\times\left(\frac{2V_sX}{kfL_sY}-2\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}+I_o\right)+$$
$$\left.+0{\cdot}0764\ \frac{R_C^2I_o}{f^2}\right\}. \qquad \ldots(17b)$$

SUMMARY OF RESULTS

Forward converter

$$\Delta V_{R(C)} = \frac{(V'_{CC}-V_s)R_CV_s}{fLV'_{CC}}$$

$$\Delta V_{L(C)} = V'_{CC}\frac{L_C}{L}$$

$$\Delta V_C = \frac{1}{C}\,\frac{(V'_{CC}-V_s)V_s}{8f^2LV'_{CC}}$$

$$I_{C(pk)} = \frac{(V'_{CC}-V_s)V_s}{2fLV'_{CC}}$$

$$I_{r.m.s.} = I_{C(pk)}/\sqrt{3}$$

Push-pull converter

$$\Delta V_{R(C)} = \frac{R_C(V'_{CC}-V_s)V_s}{2fLV'_{CC}}$$

$$\Delta V_{L(C)} = \frac{L_C}{L}V'_{CC}$$

$$\Delta V_C = \frac{1}{C}\,\frac{(V'_{CC}-V_s)V_s}{32f^2LV'_{CC}}$$

$$I_{C(pk)} = \frac{(V'_{CC}-V_s)V_s}{4fLV'_{CC}}$$

$$I_{r.m.s.} = I_{C(pk)}/\sqrt{3}$$

Flyback converter

$$\Delta V_{R(C)} = R_C\left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}} \qquad \text{where } X = kV'_{CC}-V_s \text{ and } Y = V'_{CC}-kV_s$$

$$\Delta V_{L(C)} = \frac{L_C}{L_s}\left(\frac{X}{(1-k^2)}+V_s\right), \quad \text{if } t_d > 0$$

$$\text{or } \Delta V_{L(C)} = \frac{2L_CkV'_{CC}}{(1-k^2)L_s}, \quad \text{if } t_d < 0$$

$$\Delta V_C = \frac{kI_oL_s}{2C}\left(\frac{1-k^2}{X}+\frac{1}{V_s}\right)\times$$
$$\times\left(\frac{2V_sX}{fL_sYk}-2\left[\frac{2V_sI_oX}{fL_sYk}\right]^{\frac{1}{2}}+I_o\right)$$

$$I_{C(pk)} = \left[\frac{2I_oV_sX}{kfL_sY}\right]^{\frac{1}{2}}-I_o$$

where V_{CC} = primary supply voltage
n = transformer turns-ratio
$V'_{CC} = V_{CC}/n$ = peak secondary open-circuit voltage
V_o = regulated output voltage
V_R = forward voltage drop of output rectifier diode
$V_s = V_o + V_R$
I_o = output current
k = transformer coupling constant (flyback converters only)
f = operating frequency

L = inductance of smoothing choke (forward and push-pull converters only)
L_s = inductance of transformer secondary winding
L_C = ESL of output filter capacitor
R_C = ESR of output filter capacitor
C = purely capacitive part of output filter capacitor

Summary of assumptions and approximations

In deriving the above relationships, the following are assumed:

a) a.c. and d.c. winding resistances and core losses in the transformer are small;
b) therefore, the rates of change of current in the transformer are governed entirely by the circuit voltages and inductances;
c) the diodes are perfect switches, with constant forward offset voltage V_R, zero reverse leakage current, and instantaneous turn-on and turn-off;
d) the transistors are perfect switches with $V_{CE(sat)} = 0$;
e) the supply voltage V_{CC} is essentially constant during one converter cycle;
f) the output ripple voltage is small compared with the output voltage, and therefore the voltage across the output capacitor is approximately constant;
g) the load is constant;
h) the power supply is in regulation equilibrium at its operating point;
i) the output filter capacitor can be represented by an equivalent series circuit consisting of resistance, inductance, and capacitance.

ANALYSIS OF LOAD REGULATION CHARACTERISTICS OF SWITCHED-MODE POWER SUPPLIES

In this Section, a brief examination is made of the response of the output filter circuit to a sudden change in load.

If the load is changed abruptly, the current in the circuit inductances cannot change rapidly enough to keep the output voltage constant. The current is thus diverted into, or out of the capacitor, which starts to charge or discharge until the current supplied to the capacitor can be adjusted by the feedback loop to compensate for the changed conditions. The voltage across the capacitor ESR will change, owing to the capacitor charging or discharging current, and the voltage on the capacitive part of the output filter capacitor will at first increase or decrease linearly with time.

If the change in output current is $-\Delta I_o$, the voltage change across the capacitor ESR is $R_C\Delta I_o$, and the voltage on the capacitive part increases as $(1/C)(\Delta I_o t)$. A voltage pulse also appears across the capacitor ESL while the load current is changing; the maximum possible value of this pulse is equal to $(V_o\Delta I_o)/(I_o-\Delta I_o)$. This pulse is derived by assuming that initially, after an instantaneous change of load, the load current is maintained at its former value by the capacitor ESL. The load current reaches its new value with a very short time-constant, $\tau = L_C/(R+\Delta R)$. In practice, the time taken for the effective load resistance to change will in general be large compared with τ, and the voltage pulse due to the capacitor ESL may be ignored.

The voltage change across the output capacitor can thus be given as:

$$\Delta V_o = \Delta I_o\left(R_C+\frac{t}{C}\right).$$

If there is a time delay t_R before the converter supply current to the output capacitor can start to change to compensate for the changed load current, the maximum change in output voltage for a change $(-\Delta I_o)$ in output current is given by:

$$\Delta V_o = \Delta I_o(R_C+t_R/C).$$

Thus, in addition to C being sufficiently large to minimize the ripple voltage, it is also necessary to have:

$$C \geqslant t_R\Big/\left(\frac{\Delta V_o}{\Delta I_o}-R_C\right)$$

where $\Delta V_o/\Delta I_o$ is the required output impedance, R_C is the ESR of the output filter capacitor, and t_R is the recovery time of the circuit.

For flyback circuits in which the transformer flux does not reach zero during the cycle, the above voltage change is not applicable. In these circuits, the transient voltage can be considerably larger than implied above, and its value depends on the individual circuit considered.

DISCUSSION OF RESULTS

A cursory examination of the results presented in the Summary of Results on p. 133 reveals several points. There is an inherent disadvantage in flyback supplies when the transformer coupling constant is low, because some of the energy stored in the core is returned to the supply rather than transmitted to the output. The amount of energy wasted is proportional to the transformer leakage inductance. However, a low coupling constant and, consequently, a large leakage inductance is required to reduce the amount of ripple voltage across the ESL of the output filter capacitor. The transformer leakage inductance is therefore the only smoothing choke in the secondary circuit.

The high peak-to-mean ratio of the transformer secondary current in the flyback circuit results in a much higher level of ripple across the capacitor ESR, compared with the forward converters and push-pull converters. There are, therefore, conflicting requirements for the transformer design, and ripple must be a compromise with efficiency.

A second point is that, from the Summary of Results on p. 133, it might be thought that the push-pull converter would have a decided advantage over the forward converter, in terms of ripple voltage. However, if the smoothing choke L in the output filter is chosen in both circuits to give the same peak diode current, then the inductance needed for the forward converter is twice that needed for the push-pull converter. Because a lower secondary voltage is required in the push-pull converter, compared with the forward converter, the ESR ripple component is the same for both circuits. The forward converter has a small advantage over the push-pull converter, in having a

slightly lower ESL ripple voltage. As will be shown, the ripple voltage developed across the purely capacitive part of the output capacitor is unimportant in this application. The capacitance value will usually be chosen from considerations of transient load change, and will be generally large enough to make the ripple voltage insignificant.

In order to use the Summary of Results on p. 133, some assumptions must be made in order to combine the ripple voltage waveforms due to the separate equivalent series components of the output capacitor. An examination of the waveforms in Figs. 2b and 9 shows that the contributions to ripple voltage due to the capacitor ESL and ESR have peak values occurring at the same time which may therefore be linearly added. The contribution of the capacitive portion is, however, out of phase with the other components, and may increase or decrease the total ripple voltage. However, if the capacitive contribution exceeds either the resistive or inductive contributions, the total ripple voltage will start to increase once more. It is consequently suggested that to calculate maximum values of L_C and R_C and minimum values of C, each of the three ripple voltage components should be separately equated to one half of the total maximum ripple permitted.

CALCULATIONS OF REQUIREMENTS FOR VARIOUS POWER SUPPLIES AND COMPARISON OF THEORY WITH OBSERVATION

Tables 1a and 1b contain the results of some calculations for four different sets of power supply output requirements, for each of the three types of SMPS, and for four different levels of ripple (p. 136).

The tables were calculated using the expressions in the Summary of Results for ripple voltage, the expressions derived on p. 134 for load regulation, and the following assumptions about general power supply design.

In both forward and push-pull power supplies, the peak rectifier current at maximum load current is 10% greater than the load current (that is, the capacitor peak-to-peak ripple current is 20% of the output current). The value of the smoothing choke is thus defined by:

$$L \geqslant 5\frac{V_o t_b}{I_o}.$$

where V_o is the output voltage, t_b is the average off-time of the transistors in the primary circuit, and I_o is the maximum output current. Substituting for t_b,

$$L \geqslant \frac{5(V'_{CC}-V_o)}{I_o f}.$$

a) For the forward converter:
The voltage V'_{CC} must be greater than twice the sum of the required output voltage and the diode voltage drop $(V_o+V_R = V_s)$ even at the lowest supply voltage; allowing a range of 225V to 400V for the rectified and smoothed 240V a.c. mains. This means that the duty cycle can vary between 28% and 50% (this also allows for missing half-cycles at minimum mains voltage, and for third-harmonic distortion and transient spikes at maximum mains voltage). Allowing for this condition, the secondary voltage at maximum possible supply voltage will be $V'_{CC} = 3{\cdot}6V_s$; this is the point at which the ripple will be a maximum.

b) For the push-pull converter:
The duty cycle can vary between 56% and 100% as the supply voltage varies over its maximum range; maximum ripple occurs at maximum mains voltage and a minimum duty cycle of 56%; that is,

$$V'_{CC} = 1{\cdot}8V_s.$$

c) For the flyback converter:
(i) The peak secondary voltage V'_{CC} at minimum supply voltage must be greater than V_s, so again
$V'_{CC} = 1{\cdot}8V_s$ at maximum ripple.
(ii) The value of the transformer secondary inductance is chosen so that at minimum supply voltage and maximum output current (that is, maximum duty cycle), the secondary current decays to zero just before the transistors in the primary circuit are turned on. Ripple is a maximum at maximum output current, and is almost independent of supply voltage.

Examination of the values of L_C and R_C derived for push-pull converters and forward converters (Table 1a and 1b) verifies the conclusions drawn in the Summary of Results on p. 133.

A closer study of Table 1 reveals some general trends. The permissible maximum values of both L_C and R_C decrease steadily as a) V_o decreases, b) I_o increases, and c) the % ripple decreases. Thus, a parameter might be used to represent the degree of difficulty in matching the required capacitor specification for a particular power supply with a practical capacitor. Such a parameter is arbitrarily defined as:

$$D = I_o/\Delta V_o,$$

where ΔV_o is the peak-to-peak output ripple voltage, or:

$$D = \frac{100I_o}{rV_o},$$

where r is the % ripple voltage ($r = 100\Delta V_o/V_o$).

If the maximum permissible values of L_C and R_C are plotted as a function of D for a wide range of different power supply specifications, the resulting graphs show that for a particular type of power supply both L_C and R_C are almost exactly proportional to 1/D. On a log-log scale, the graph for each type of SMPS becomes a straight line with a slope of -1 (see Figs. 13 and 14).

It can readily be seen from Figs. 13 and 14 that flyback supplies require smaller values of L_C and R_C than the push-pull and forward supplies. From the equations in the Summary of Results, straight lines might be expected for the forward and push-pull converters. The straight lines obtained for flyback converters are the results of assumptions made in designing the power supply output stages.

From observations of the graphs in Figures 13 and 14 for any given capacitor ESL and ESR, the maximum

TABLE 1a

Output filter parameters for various power supplies (transient change = 10× peak-to-peak ripple)

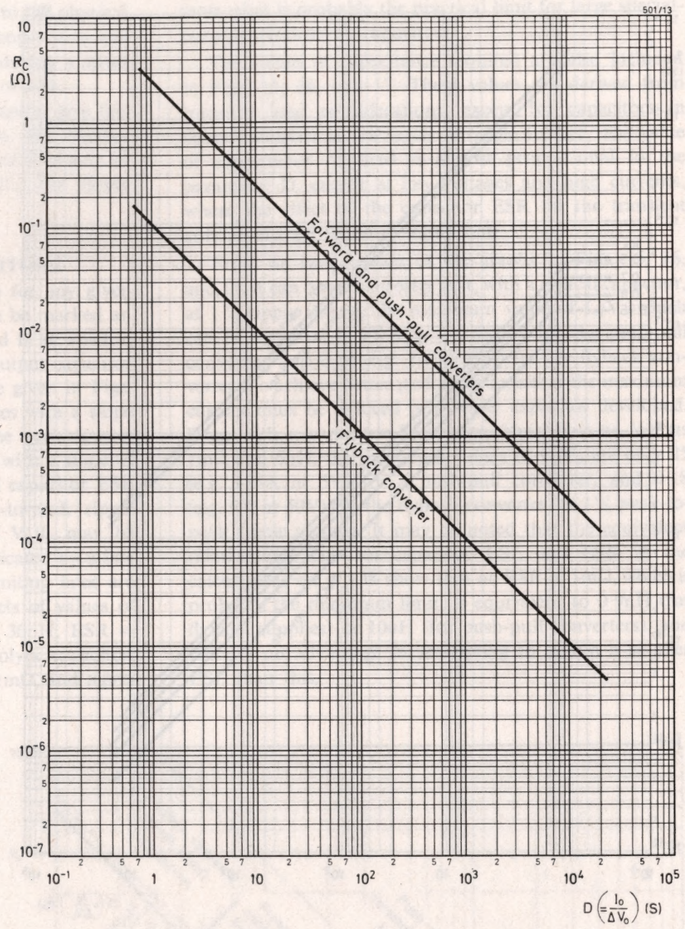
Ripple		0·1%				0·3%			
Type of Supply	V_o I_o	50V 1A	50V 10A	5V 10A	5V 100A	50V 1A	50V 10A	5V 10A	5V 100A
FLYBACK	$L_s =$	134·5μH	13·45μH	1·489nH	148·9nH	134·5μH	13·45μH	1·489μH	148·9nH
$1{\cdot}1V_s \leqslant kV'_{CC} \leqslant 2V_s$	$C \geqslant$	163μF	1·63mF	16·3mF	175mF	54·0μF	540μF	5·40mF	54·6mF
$k = 0{\cdot}95$	$R_C \leqslant$	4·89mΩ	489μΩ	48·9μΩ	4·89μΩ	14·7mΩ	1.47mΩ	147μΩ	14·7μΩ
$f = 25kHz$	$L_C \leqslant$	5·91nH	591pH	59·1pH	5·91pH	17·7nH	1·77nH	177pH	17·7pH
	$I_{pk} =$	4·10A	41·03A	41·03A	410·3A	4·10A	41·03A	41·03A	410·3A
FORWARD	$L =$	7·31mH	731μH	80·9μH	8·09μH	7·31mH	731μH	80·9μH	8·09μH
$2V_s \leqslant V'_{CC} \leqslant 3{\cdot}6V_s$	$C \geqslant$	163μF	1·63mF	16·3mF	175mF	54·0μF	540μF	5·40mF	54·6mF
$f = 25kHz$	$R_C \leqslant$	125mΩ	12·5mΩ	1·25mΩ	125μΩ	375mΩ	37·5mΩ	3·75mΩ	375μΩ
	$L_C \leqslant$	1·00μH	100nH	10·0nH	1·00nH	3·00μH	300nH	30nH	3·0nH
	$I_{r.m.s.} =$	58mA	580mA	580mA	5·8A	58mA	580mA	580mA	5·8A
PUSH-PULL	$L =$	2·25mH	225μH	24·9μH	2·49μH	2·25mH	225μH	24·9μH	2·49μH
$V_s \leqslant V'_{CC} \leqslant 1{\cdot}8V_s$	$C \geqslant$	163μF	1·63mF	16·3mF	175mF	54·0μF	540μF	5·40mF	54·6mF
$f = 25kHz$	$R_C \leqslant$	125mΩ	12·5mΩ	1·25mΩ	125μΩ	375mΩ	37·5mΩ	3·75mΩ	375μΩ
	$L_C \leqslant$	1·23μH	123nH	12·3nH	1·23nH	3·70μH	370nH	37nH	3·7nH
	$I_{r.m.s.} =$	58mA	580mA	580mA	5·8A	58mA	580mA	580mA	5·8A

TABLE 1b

Output filter parameters for various power supplies (transient change = 10× peak-to-peak ripple)

Ripple		1%				3%			
Type of Supply	V_o I_o	50V 1A	50V 10A	5V 10A	5V 100A	50V 1A	50V 10A	5V 10A	5V 100A
FLYBACK	$L_s =$	134·5μH	13·45μH	1·489μH	148·9nH	134·5μH	13·45μH	1·489μH	148·9nH
$1{\cdot}1V_s \leqslant kV'_{CC} \leqslant 2V_s$	$C \geqslant$	16·3μF	163μF	1·63mF	16·3mF	5·40μF	54·0μF	540μF	5·40mF
$k = 0{\cdot}95$	$R_C \leqslant$	48·9mΩ	4·89mΩ	489μΩ	48·9μΩ	147mΩ	14·7mΩ	1·47mΩ	147μΩ
$f = 25kHz$	$L_C \leqslant$	59·1nH	5·91nH	591pH	59·1pH	177nH	17·7nH	1·77nH	177pH
	$I_{pk} =$	4·10A	41·03A	41·03A	410·3A	4·10A	41·03A	41·03A	410·3A
FORWARD	$L =$	7·31mH	731μH	80·9μH	8·09μH	7·31mH	731μH	80·9μH	8·09μH
$2V_s \leqslant V'_{CC} \leqslant 3{\cdot}6V_s$	$C \geqslant$	16·3μF	163μF	1·63mF	16·3mF	5·40μF	54·0μF	540μF	5·40mF
$f = 25kHz$	$R_C \leqslant$	1·25Ω	125mΩ	12·5mΩ	1·25mΩ	3·75Ω	375mΩ	37·5mΩ	3·75mΩ
	$L_C \leqslant$	10·0μH	1·00μH	100nH	10nH	30·0μH	3·00μH	300nH	30·0nH
	$I_{r.m.s.} =$	58mA	580mA	580mA	5·8A	58mA	580mA	580mA	5·8A
PUSH-PULL	$L =$	2·25mH	225μH	24·9μH	2·49μH	2·25mH	225μH	24·9μH	2·49μH
$V_s \leqslant V'_{CC} \leqslant 1{\cdot}8V_s$	$C \geqslant$	16·3μF	163μF	1·63mF	16·3mF	5·40μF	54·0μF	540μF	5·40mF
$f = 25kHz$	$R_C \leqslant$	1·25Ω	125mΩ	12·5mΩ	1·25mΩ	3·75Ω	375mΩ	37·5mΩ	3·75mΩ
	$L_C \leqslant$	12·3μH	1·23μH	123nH	12·3nH	37·0μH	3·70μH	370nH	37·0nH
	$I_{r.m.s.} =$	58mA	580mA	580mA	5·8A	58mA	580mA	580mA	5·8A

Fig. 13—Maximum ESR of capacitor



possible value of D may be found; thus, if the required output voltage and current are known, the ripple voltage which will occur can be found.

a) For example, using a capacitor which has values of ESL ≃ 40nH and ESR ≃ 5mΩ, the maximum possible values of D are:

1) Flyback converter:
from ESR curve, D ⩽ 22;
from ESL curve, D ⩽ 3;
and the smaller value must be considered (D ⩽ 3).
It can be seen that D is limited by the ESL of 40nH.

2) Forward and push-pull converters:
from ESR curves, D ⩽ 500;
from ESL curves, D ⩽ 600;
so that D is limited to 500 by the ESR of 5mΩ.

b) For a second example, a capacitor representing what is probably the practical limit for large electrolytic capacitors is considered, with ESL = 6nH and ESR = 1mΩ.

1) Flyback converter:
from ESR curve, D ⩽ 110;
from ESL curve, D ⩽ 20;
so that D is limited to 20 by the ESL of 6nH.

2) Forward and push-pull converter:
from ESR curve, D ⩽ 2500;
from ESL curve, D ⩽ 4000;
so that D is limited to 2500 by the ESR of 1mΩ.

c) As a third example, a practical capacitor is considered with ESL = 15nH, ESR = 2mΩ. For this capacitor:

1) Flyback converter:
from ESR curve, D ⩽ 55;
from ESL curve, D ⩽ 8;
so that D is limited to 8 by the ESL of 15nH.

2) Forward and push-pull converter:
from ESR curve, D ⩽ 1250;
from ESL curve, D ⩽ 1700;
so that D is limited to 1250 by the ESR of 2mΩ.

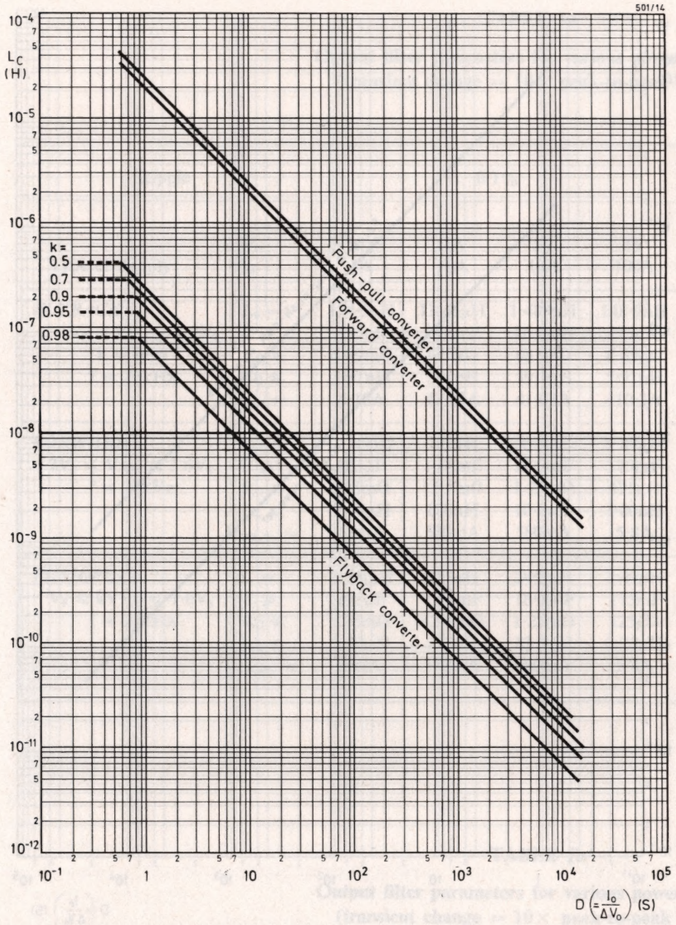


Fig. 14—Maximum ESL of capacitor

d) It might also be noted that for each type of power supply, a correspondence exists between values of ESL and ESR which gives similar ripple voltages:

1) Flyback converter:
$ESL = 0{\cdot}9 \times 10^{-6} \times ESR$ (ESL in henries, ESR in ohms).

2) Push-pull converter:
$ESL = 1 \times 10^{-5} \times ESR$.

OBSERVATIONS MADE OF THREE WORKING SWITCHED-MODE POWER SUPPLIES

Push-pull converter, 5V, 40A

From measurements of the ripple voltage waveform at full load, $\Delta V_{L(C)} = 25mV$, $\Delta V_{R(C)} = 25mV$, ΔV_C being too small to measure. The output filter capacitor was rated at 10mF and 16V. Calculations from the observed ripple voltage gave ESL = 80nH and ESR = 20mΩ; these values compare favourably with the values of impedance quoted in capacitor data, which are 20mΩ at 100kHz and 100mΩ at 100Hz.

Flyback converter, 5V, 4A

The output capacitance was made up of three 4·7mF, 10V capacitors. The observed ripple voltages were $\Delta V_{L(C)} = 50mV$, $\Delta V_{R(C)} = 200mV$. The latter voltages give values of $L_C \simeq 33nH$ and $R_C \simeq 20m\Omega$ for each capacitor. These figures are to be compared with the values quoted in the data for the capacitors, which gives impedances of 450mΩ at 100Hz and 20mΩ at 100kHz.

Push-pull converter, 5V, 100A

The output capacitor of this power supply had ratings of 100mF, 10V. Measured values of ripple voltage were $\Delta V_{L(C)} = 88mV$, $\Delta V_{R(C)} = 20mV$. For these values, $L_C = 62nH$ and $R_C = 3{\cdot}9m\Omega$. The values deduced from the data for this capacitor are 40nH and 4·5mΩ.

It can readily be seen that the ESR figures are very similar, but there is an error of about 20nH in the measurement of ESL. The error may be attributed to the physical circuit configuration, in which 200mm of copper strip was included in series with the capacitor, introducing a series inductance comparable to the error value of ESL.

In general, for all these examples, the figures give fair agreement between theory and observation; the discrepancies being attributed to circuit layout and to errors of measurement (which are generally ±10% for ripple measurements).

CHOICE OF OUTPUT FILTER CAPACITORS

A graph of V_o against I_o may be plotted for any given levels of ripple voltage. On this graph can be marked an area corresponding to the values of V_o and I_o at which a given type of converter with a particular output capacitor can be used. Examples of such graphs are given in Figs. 15, 16, and 17. On these graphs, solid lines with a slope of −1 represent constant power, limiting the working zone to between 25VA and 500VA. Solid lines with a slope of +1 represent constant V_o/I_o. For a given capacitor ESL and ESR, and a given maximum peak-to-peak ripple voltage, the minimum possible value of V_o/I_o may be found for each type of converter, and indicated by a line on the graph of V_o against I_o. These limiting lines are shown in Figs. 15, 16, and 17 for two sets of values of ESR and ESL. The first set has ESL = 30nH, ESR = 10mΩ, and represents a typical large electrolytic capacitor. The second set has ESL = 6nH, ESR = 1mΩ, and represents what is probably the practical limit for large special-purpose electrolytic capacitors.

The values of capacitance required are also included in Figs. 15, 16, and 17. These values are derived from transient load considerations, except for capacitors in flyback supplies at low levels of ripple voltage. The value of capacitance required is almost proportional to the parameter D, except at low voltages and high currents, where the effect of the capacitor ESR on the transient voltage change becomes significant.

From an examination of the graphs in Figs. 15, 16, and 17, it can be seen directly that, with a typical capacitor, at 1% ripple voltage the maximum value of I_o/V_o which can be achieved is 0·8 (e.g. 4A at 5V) for the push-pull converter, and 0·04 (e.g. 2A at 50V) for the flyback converter. To achieve better performance, either the maximum current must be reduced or a better capacitor developed. Even with a capacitor having an impedance as low as 1mΩ and 6nH, the maximum values of I_o/V_o are only 25 (e.g. 125A at 5V) for a push-pull converter, and 0·18 (e.g. 9A at 50V) for the flyback converter, at 1% peak-to-peak ripple voltage. It may be noted that the equivalent relationships between capacitor ESL and ESR in the calculations on p. 138 show that an ESR of 1mΩ, which is probably the minimum limit, is equivalent to 0·9nH (for flyback supplies) or 10nH (for push-pull converters), and there is no advantage in attempting to obtain a smaller ESL than this.

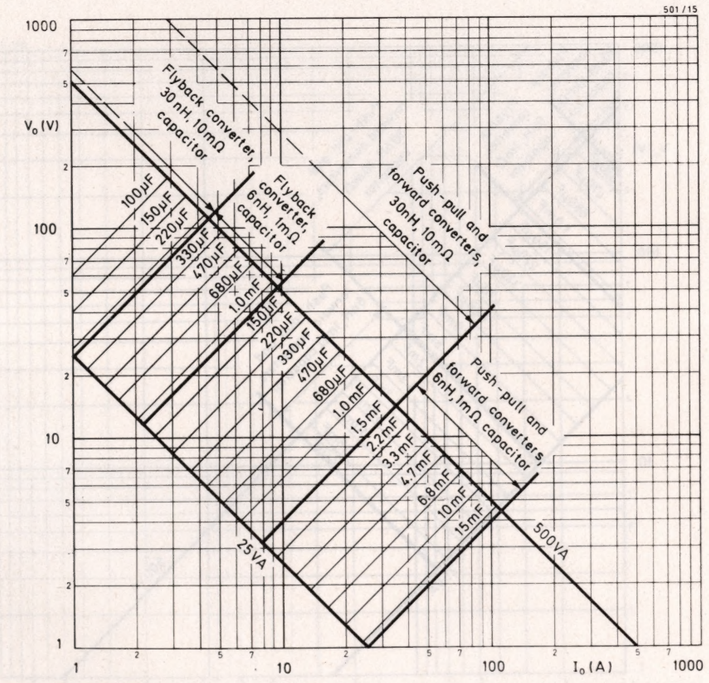


Fig. 15—1% peak-to-peak ripple (10% transient voltage change for 10% load change)

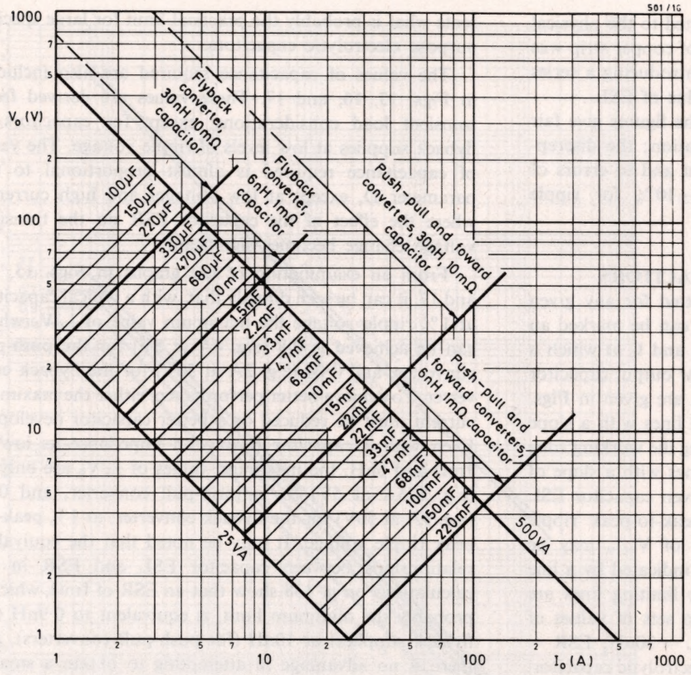


Fig. 16—1% peak-to-peak ripple (1% transient voltage change for 10% load change)

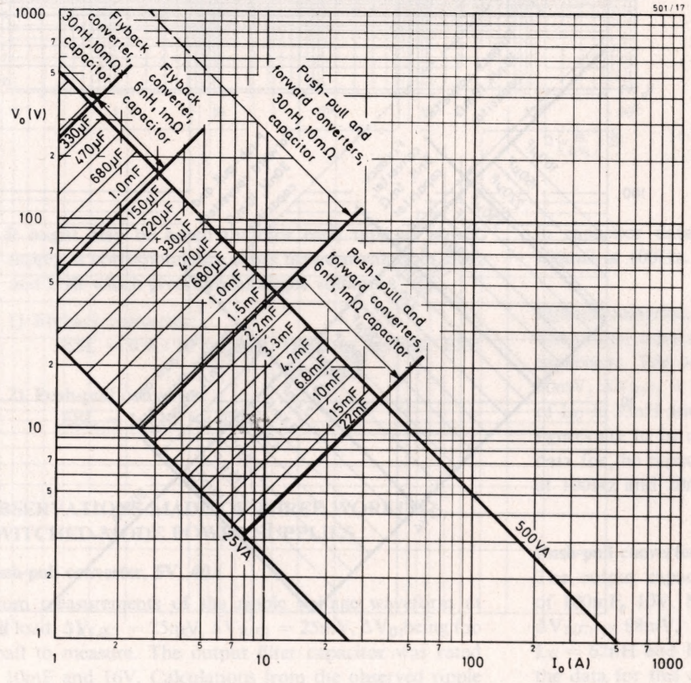


Fig. 17—0·1% peak-to-peak ripple (1% transient voltage change for 10% load change)